

WV-4 SIT LOGIC SCHEMATICS

WV-4
6/27/2016

- 001.TITLE PAGE

002.POWER SEQUENCE

003.CPU(1/16) : DDI/EDP

004.CPU(2/16) : DDR4

005.CPU(3/16) : DDR4

006.CPU(4/16) : MISC/JTAG

007.CPU(5/16) : LPC/SPI/SMBUS/C-LINK

008.CPU(6/16) : LPSS/ISH

009.CPU(7/16) : AUDIO/SDXC

010.CPU(8/16) : PCIE/USB/SATA

011.CPU(9/16) : CSI-2/EMMC

012.CPU(10/16) : CLOCK SIGNALS

013.CPU(11/16) : SYSTEM PM

014.CPU(12/16) : CPU POWER

015.CPU(13/16) : CPU POWER

016.CPU(14/16) : PCH POWER

017.CPU(15/16) : GND

018.CPU(16/16) : CFG/RESERVED

019.XDP CONNECTOR

020.RTC BATTERY

021.SPI FLASH

022.DDR4 SO DIMM

023.TYPE_C_CONTROLLER

024.TYPE-C_MUX

025.BLANK

026.BLANK

027.BLANK

028.DP SWITCH

029.DP DEMUX

030.BLANK

031.BLANK

032.BLANK

033.BLANK

034.BLANK

035.BLANK
- 036.BLANK

037.RF COMPONENT

038.LCD/LID/MIC/CAMERA/PWR SW

039.BLANK

040.HDMI CONNECTOR

041.DISPLAY PORT CONNECTOR

042.BLANK

043.SATA HDD CONN

044.USB POWER/CONN

045.USB POWER/CONN

046.GBE CLARKVILLE

047.GBE LAN SWITCH

048.GBE MAGNETICS

049.RJ45 CONNECTOR

050.PCIE MINI CARD SLOT

051.MEDIA CARD CONTROLLER

052.MEDIA CARD INTERFACE

053.SMART CARD I/F

054.AUDIO ALC3245-GRT

055.AUDIO CONNECTOR

056.AUDIO JACK SENSE

057.AUDIO EXT MIC I/F

058.AUDIO SPEAKER

059.AUDIO BEEP

060.DOCKING CONNECTOR

061.MEC1653(1/3)

062.MEC1653(2/3)

063.MEC1653(3/3)

064.KEYBOARD/TRACK POINT

065.TOUCH PAD/NFC/FPR

066.BLANK

067.FAN CONNECTOR

068.G-SENSOR

069.TPM

070.SMBUS SW/LPC DEBUG PORT
- 071.THINK ENGINE(1/2)

072.THINK ENGINE(2/2)

073.DC-IN

074.BATTERY INPUT

075.BATTERY CHARGER(BQ25700)

076.BLANK

077.BLANK

078.DC/DC VCC5M/VCC3M(TPS51285B)

079.DC/DC IMVP8(NCP81208)

080.DC/DC CPUCORE(NCP81382)

081.DC/DC VCCGFXCORE_I(NCP81381)

082.DC/DC VCCSA(NCP81380)

083.DC/DC VCC1R0_SUS(TPS51367R)

084.BLANK

085.DC/DC VCC1R2A(TPS51716)

086.DC/DC VCC1R8_SUS(RT8068A)

087.BLANK

088.DC/DC VCC2R5A(RT8068A)

089.BLOCK DIAGRAM

090.BLANK

091.BLANK

092.LOAD SW PCH SUS/TRACK POINT

093.LOAD SW LAN

094.LOAD SW CPU

095.LOAD SW B

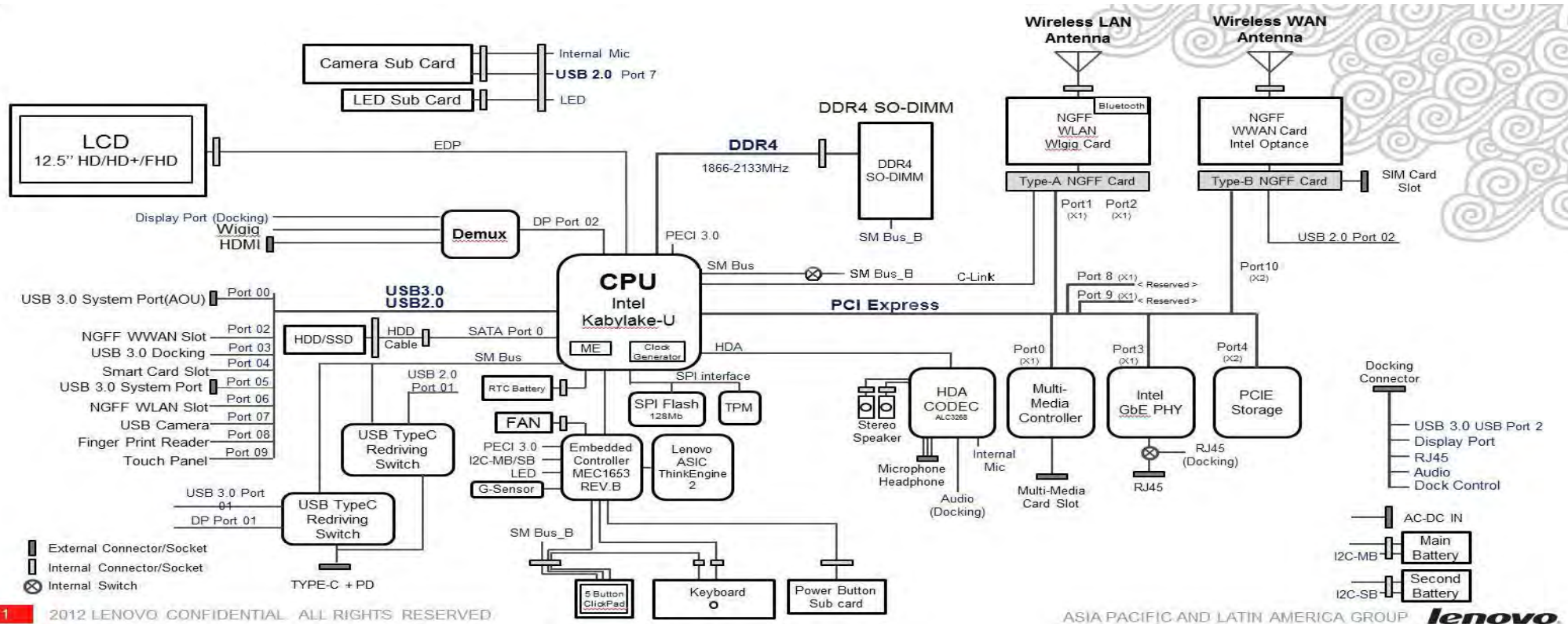
096.LOAD SW WWAN & WLAN

097.BLANK

098.PTH FOR SCREW HOLES

099.BLOCK DIAGRAM

100.NEC LED BOARD



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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane	VSYS	VCC3M	VCC1R2A	State
	VCC3SW	VCC5M		
				VCC1R0_SUS(Deep Sleep) VCC3B VCCST_CPU(Deep Sleep) VCCSTG_CPU +VCCSA VCCCFUIO VCCCFUCORE VCC1R8_SUS(Deep Sleep) VCC3_SUS(Deep Sleep) VCCMPHY_GATE VCCGFXCORE_I VCCSTG
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

EC SMBus1 address EC SMBus2 address

Device	Address	Device	Address
G-Sensor (KX023)	0011 110Xb	BATTERY Charger PU101	0x12H (0001001bX)

PCH SM Bus address PCH SM Bus0 address

Device	Address	Device	Address
CH-A DDR DIMMO (J21)	1001 0000b	Intel Lan_J219	0XC8
Touch Pad	\$2C	NFC	?????

EC SMBus0 address EC SMBus7 address

Device	Address	Device	Address
Main Battery	0x16	Second Battery	0 X16

EC SMBus5 address

Device	Address
Type C controller	000B

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
I3@	CPU I3 KABylake U
I5@	CPU I5 KABylake U
I7@	CPU I7 KABylake U
VPRO@	For VPRO part
NVPRO@	For NVPRO part
TI@	For TI TUSB546 Type C Switch
PA@	For Parade 8743 Type C Switch
ME@	ME part(connector, hole)
CONN@	ME part(connector, hole)
RF@	RF component
RF NS@	RF reserved components
EMC NS@	EMC reserved components
EMC@	EMC components
KABYU@	For Kabylake use
SKYU@	For skylake U use
SKYI3@	CPU I3 SKYlake U
SKYI5@	CPU I5 SKYlake U
SKYI7@	CPU I7 SKYlake U
SKYI5 VPRO@	For I5 VPRO SKYLAKE CPU
SKYI7 VPRO@	For I7 VPRO SKYLAKE CPU
i5 VPRO@	For I5 VPRO KABYLAKE CPU
i7 VPRO@	For I7 VPRO KABYLAKE CPU

CPU

PCB

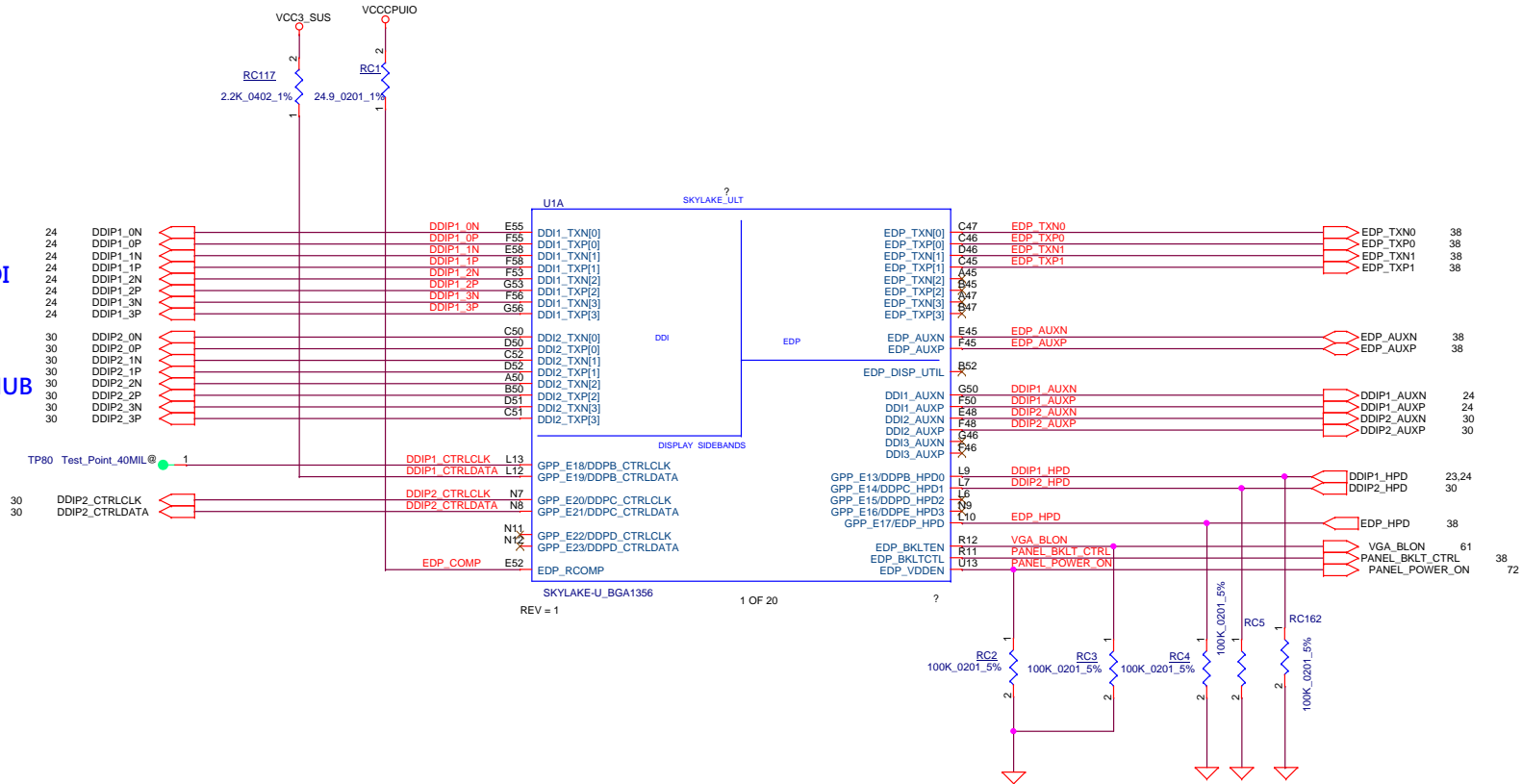
ZZZ

NM-B061

DAZ12F00100

Type C DDI

1 to 3 DP HUB



S IC FJ8067702739738 SR2ZW H0 2.4G 01 I, A.5
SA000080720
I3@



S IC FJ8067702739739 SR2ZU H0 2.5G 01 I, A.4
SA000080320
I5@



S IC FJ8067702739740 SR2ZV H0 2.7G 01 I, A.4
SA000080420
I7@



S IC FJ8067702739633 SR340 H0 2.6G 01 I, A.3
SA000086M10
I5 VPRO@



S IC FJ8067702739628 SR33Z H0 2.8G 01 I, A.3
SA000086N10
I7 VPRO@



S IC FJ8066201931106 QLB3 D1 2G BGA 1356, A.3
SA000082E20
SKYI3@



S IC FJ8066201930409 SR2EY D1 2.3G 01 I, A.3
SA00007GP30
SKYI5@



S IC FJ8066201930408 SR2EZ D1 2.5G 01 I, A.3
SA00007GM30
SKYI7@



S IC FJ8066201924931 SR2F0 D1 2.4G BGA 1356 01 I, A.3
SA00007GN20
SKYI5 VPRO@



S IC FJ8066201924950 SR2F1 D1 2.6G 01 I, A.5
SA00007GL30
SKYI7 VPRO@

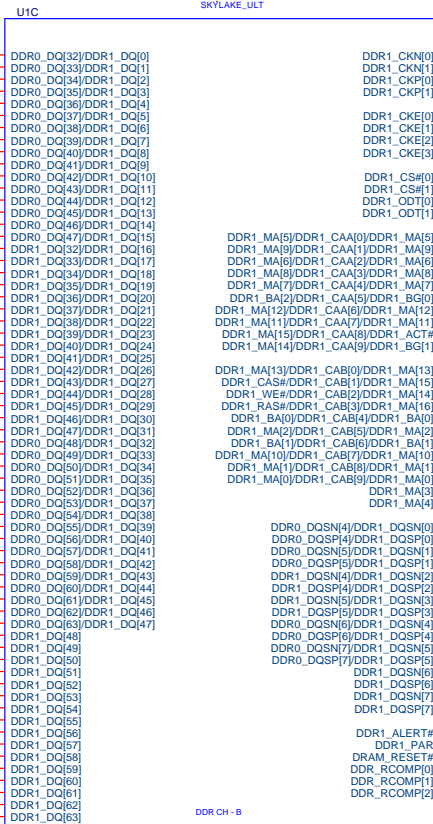
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TABLE			
	Pin	Interleave	Non-Interleave
Block 1	AF66	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK66	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF68	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK68	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF69	DDR1_DQ[9]	DDR0_DQ[25]
	AK71	DDR1_DQ[10]	DDR0_DQ[26]
	AK68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AK70	DDR1_DQ[14]	DDR0_DQ[30]
	AK68	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[32]
	AU66	DDR1_DQ[17]	DDR0_DQ[33]
	AP66	DDR1_DQ[18]	DDR0_DQ[34]
	AN66	DDR1_DQ[19]	DDR0_DQ[35]
	AN68	DDR1_DQ[20]	DDR0_DQ[36]
	AT66	DDR1_DQ[21]	DDR0_DQ[37]
	AT66	DDR1_DQ[22]	DDR0_DQ[38]
	AU66	DDR1_DQ[23]	DDR0_DQ[39]
	AT61	DDR1_DQ[24]	DDR0_DQ[40]
	AU61	DDR1_DQ[25]	DDR0_DQ[41]
	AP60	DDR1_DQ[26]	DDR0_DQ[42]
	AN60	DDR1_DQ[27]	DDR0_DQ[43]
	AN61	DDR1_DQ[28]	DDR0_DQ[44]
	AP61	DDR1_DQ[29]	DDR0_DQ[45]
	AT60	DDR1_DQ[30]	DDR0_DQ[46]
	AU60	DDR1_DQ[31]	DDR0_DQ[47]
Block 5	AU46	DDR1_DQ[32]	DDR1_DQ[16]
	AT46	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR46	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU36	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP38	DDR1_DQ[45]	DDR1_DQ[29]
	AR36	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[48]
	AT26	DDR1_DQ[50]	DDR1_DQ[50]
	AU26	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN26	DDR1_DQ[54]	DDR1_DQ[54]
	AP26	DDR1_DQ[55]	DDR1_DQ[55]
	AT25	DDR1_DQ[56]	DDR1_DQ[56]
	AU25	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

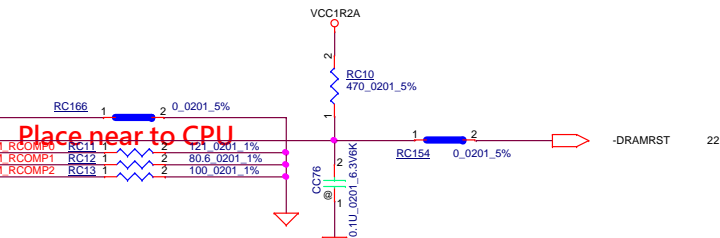
TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]



TABLE

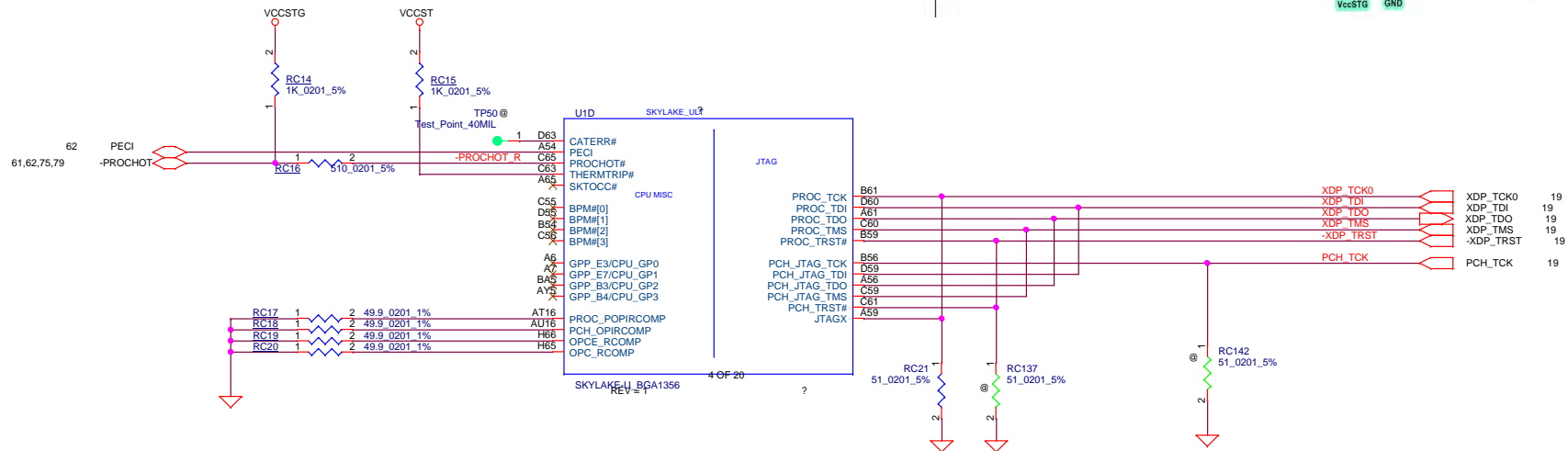
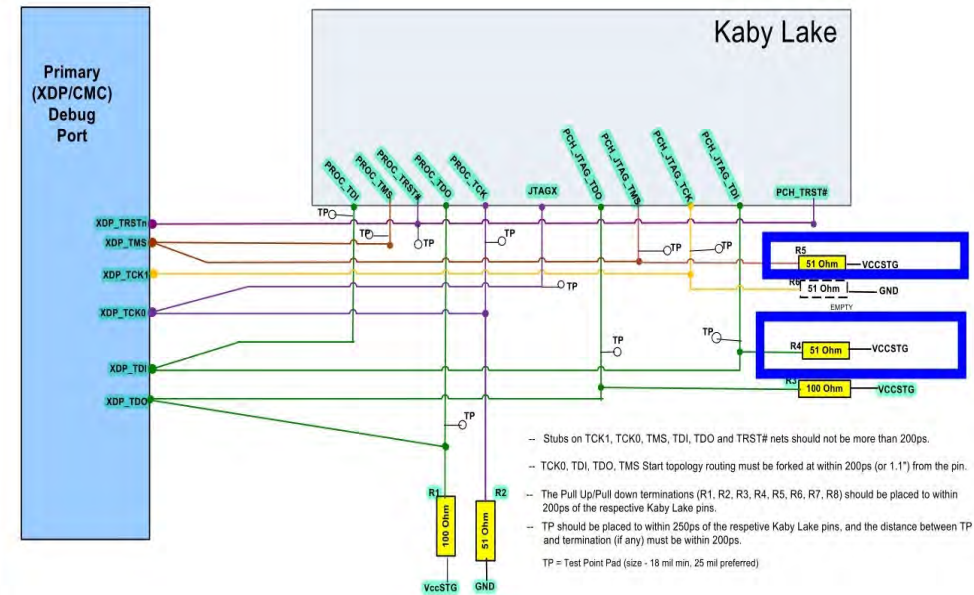
Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]




Update description

For DCI debug
 RC113 OP, RC148 short(XDP_TDO→ PCH_TDO)
 RC138 OP, RC145 short(XDP_TMS→ PCH_TMS)
 RC137 OP, RC147 short(XDP_TRST→ PCH_TRST)
 RC142 OP, RC143 short(XDP_TCK0→ JTAGX)
 RC139 OP, RC146 short(XDP_TDI→ PCH_TDI)

Figure 43-1. Primary Debug Port-JTAG Topology for Dual Scan Chain Only Design



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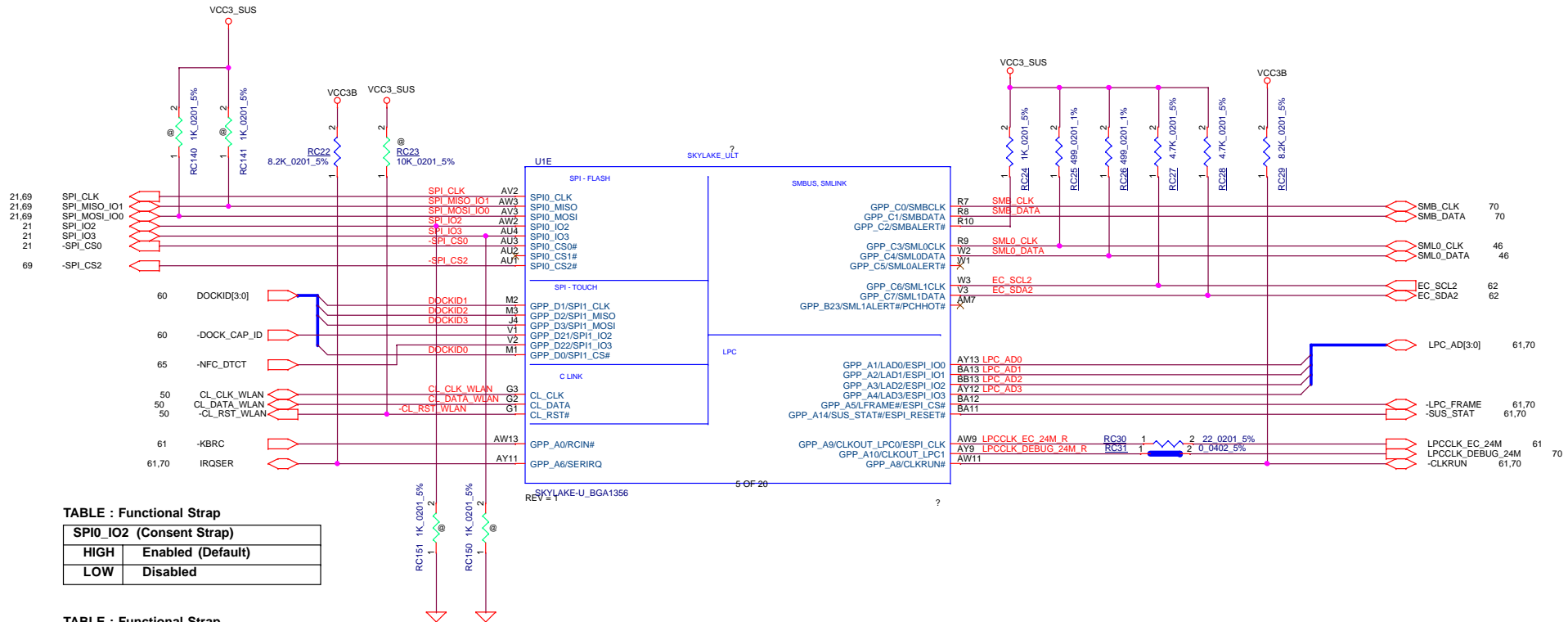


TABLE : Functional Strap

SPI0_I02 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap

SPI0_I03 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

TABLE : Functional Strap

SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

TABLE : Functional Strap

SPI0_MISO (JTAG ODT Disable)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

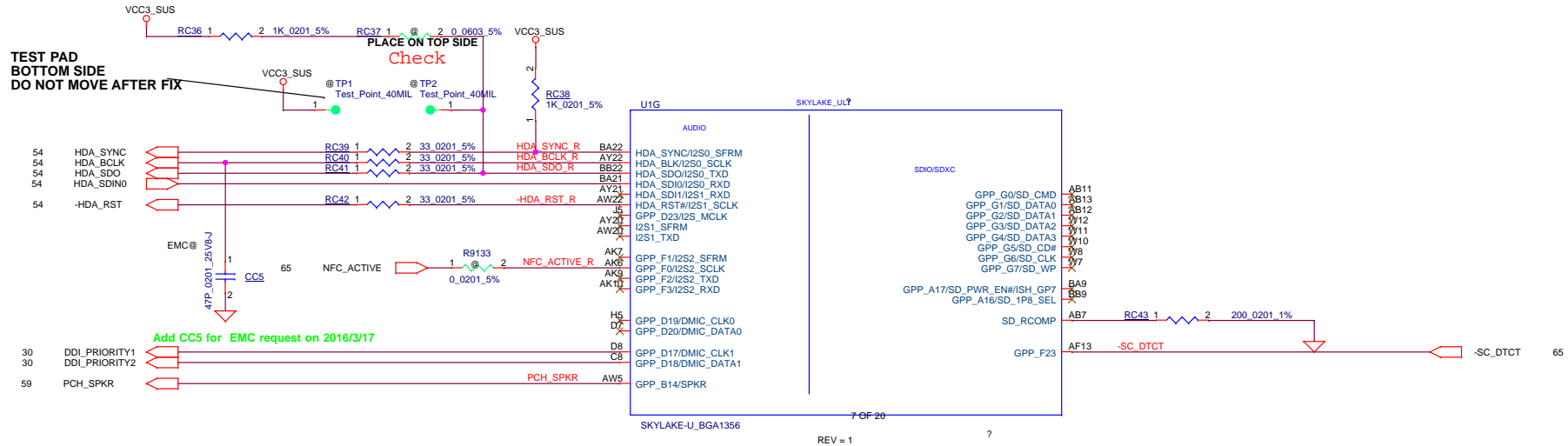
TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

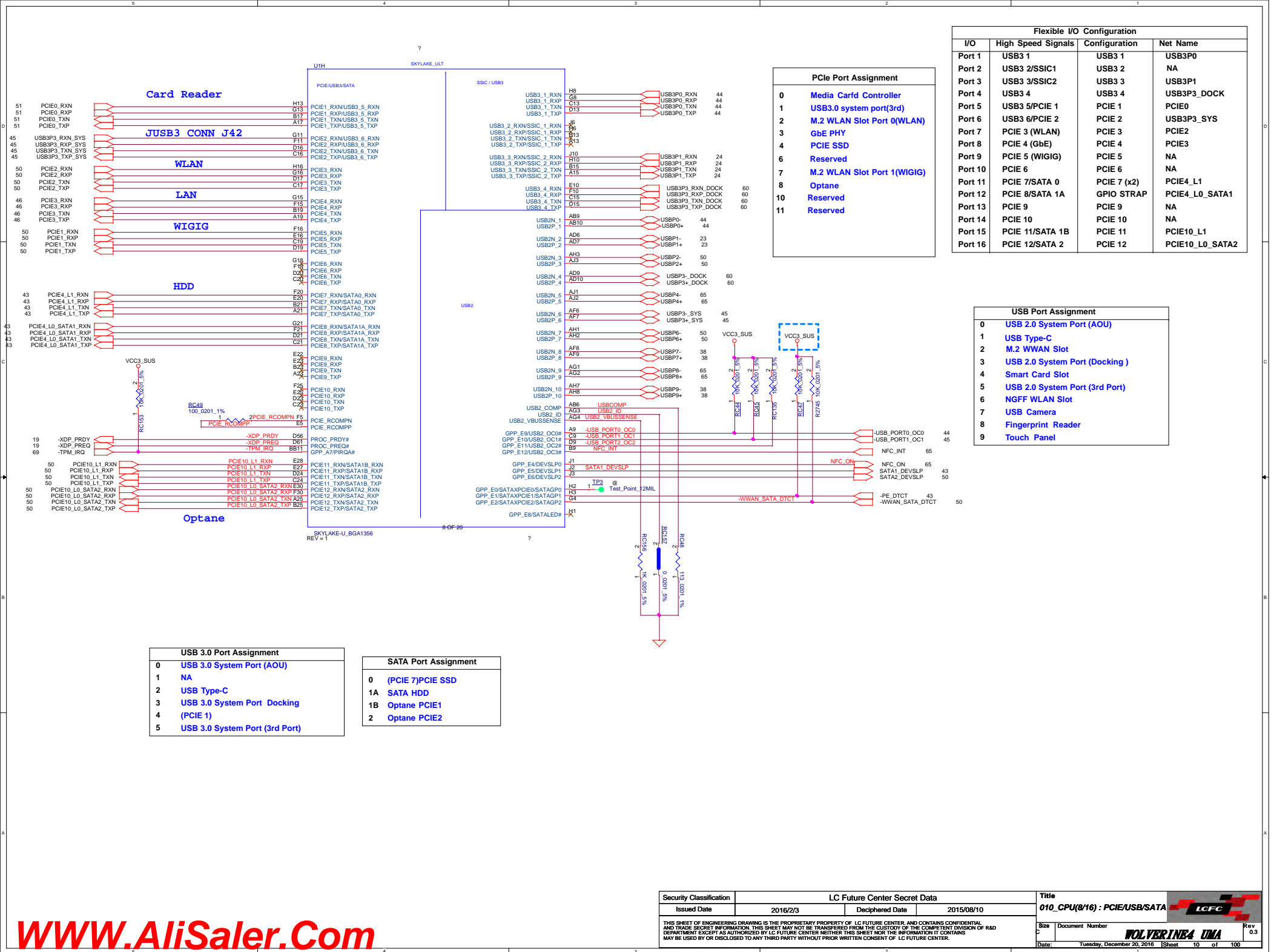
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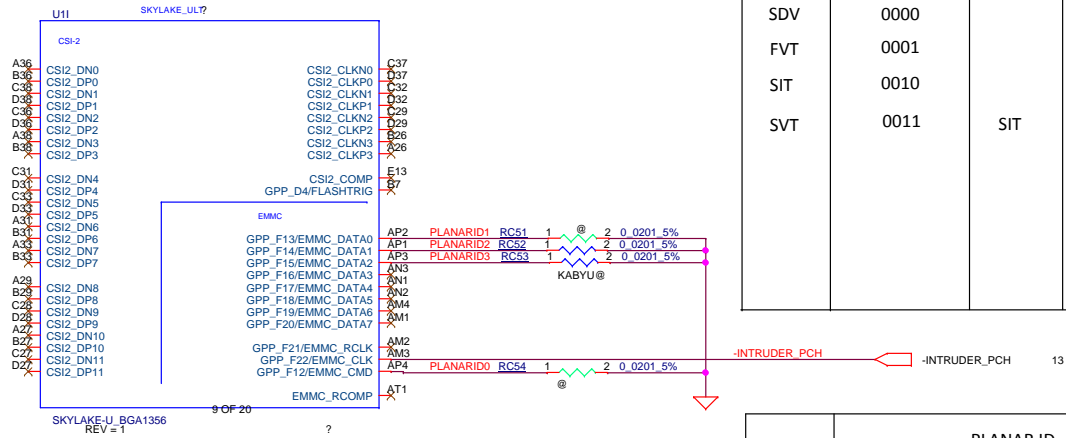
HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



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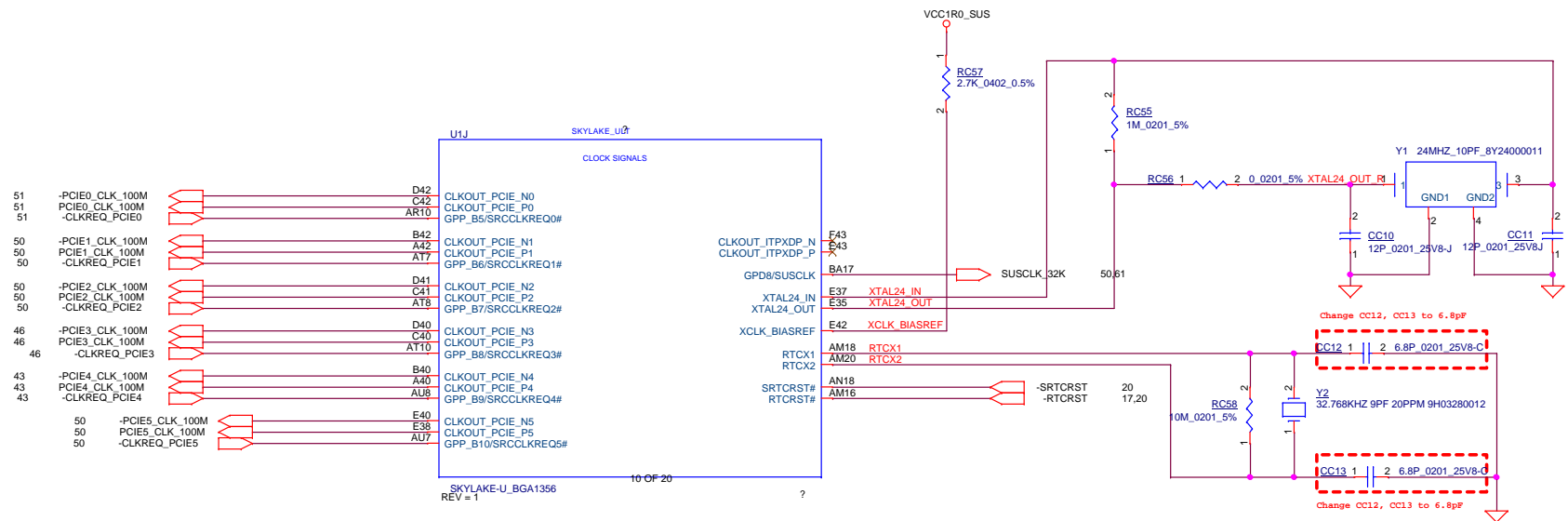
Title		LCFC	
CPU(7/16) : AUDIO/SDXC			
Size	Document Number	Rev	0.3
Custom			
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Kabylake	PLANAR ID[3..0]	SKYLAKE	PLANAR ID[3..0]
SDV	0000		
FVT	0001		
SIT	0010		
SVT	0011	SIT	1011

LEVEL	PLANAR ID			
	3	2	1	0
	RC53	RC52	RC51	RC54
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM



Y2 32.768KHZ

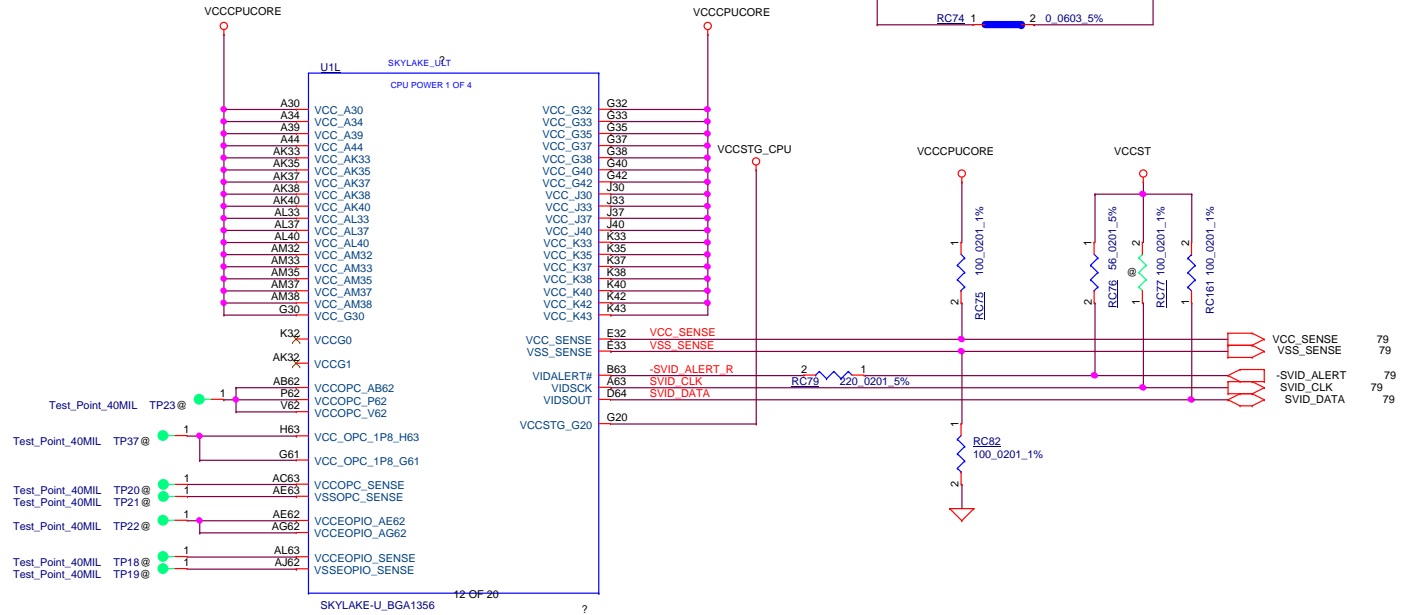
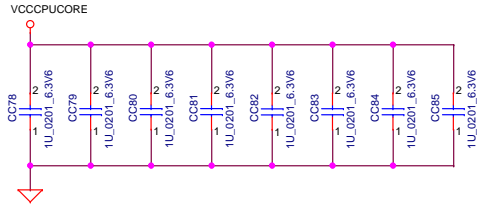
Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
KDS	50K ohm Max	SJ100069400	1TJF090DJ1A000B	50K ohm Max
SEIKO	50K ohm Max	SJ10000IX00	X1A000141000200	50K ohm Max
TXC	50K ohm Max	SJ10000J900	9H3280012	50K ohm Max

Y1 24MHZ

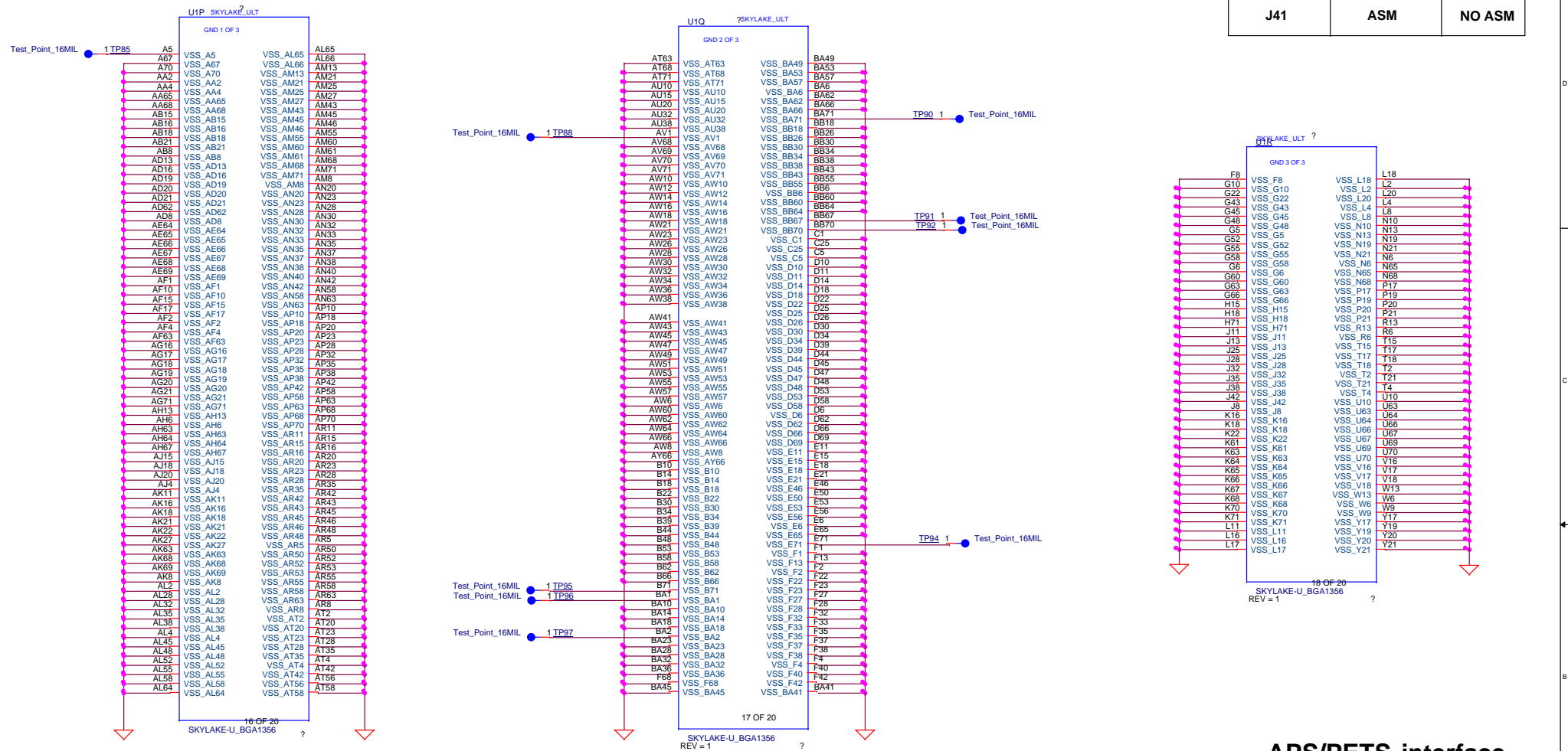
Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
TXC	50 ohm Max	SJ10000HH0J	8Y24000011	50 ohm Max
KDS	50 ohm Max	SJ10000P100	1ZZHAE24000BC0D	50 ohm Max

Security Classification	LC Future Center Secret Data			Title
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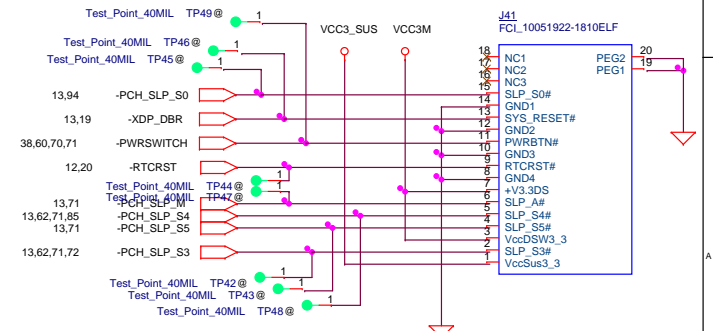
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CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM

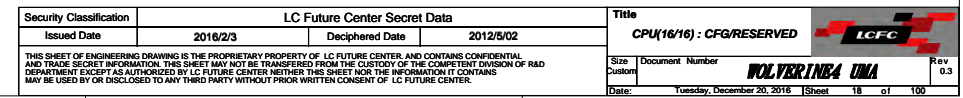


APS/PETS interface



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<p>CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall</p>
<p>CFG4 : eDP Enable 1 : Disabled 0 : Enabled</p>
<p>CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled</p>



-XDP_DBR Pull Up 10k to VCC3_SUS on 2016/3/17

Pull up TMS & TDI to VCCSTG on 2016/3/11

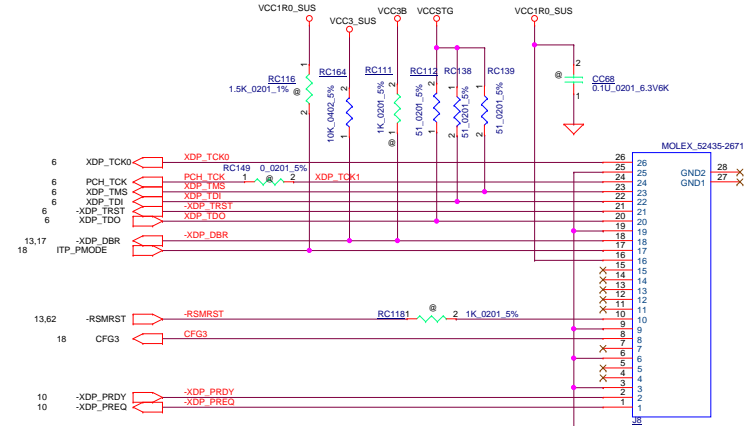


TABLE: CPU ITP DEBUG PORT

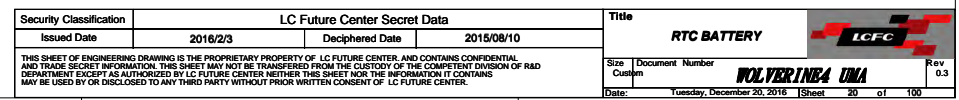
SIGNAL	REF DES	Planar only	BOX
TDO	RC109	ASM	ASM
TRST#	RC113	ASM	ASM
DBRST#	RC110	ASM	ASM
RESET#	RC111	ASM	ASM
PWRGD	RC112	ASM	ASM
CONNECTOR	J8	ASM	NO ASM

NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

TABLE: PCH ITP DEBUG port

SIGNAL	REF DES	Planar only	BOX
TDO	RC114	ASM	ASM
TMS	RC116	ASM	ASM
TDI	RC115	ASM	ASM
TCK	RC117	ASM	ASM
CPUCORE_PWRGD	RC118	ASM	ASM
-RSMRST	RC119	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV



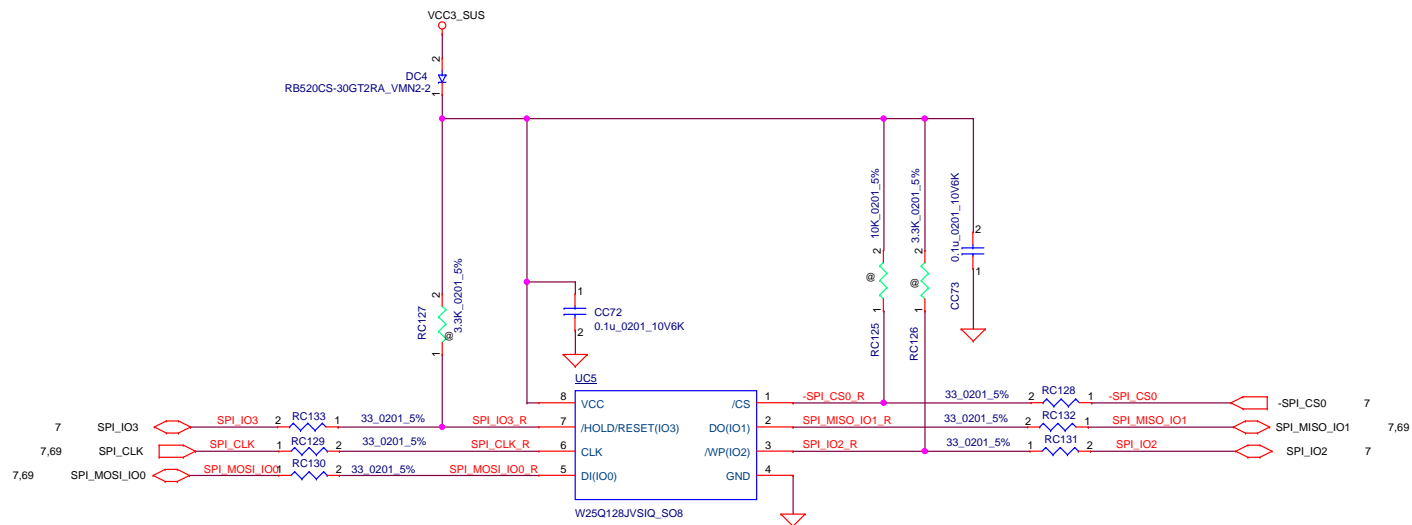
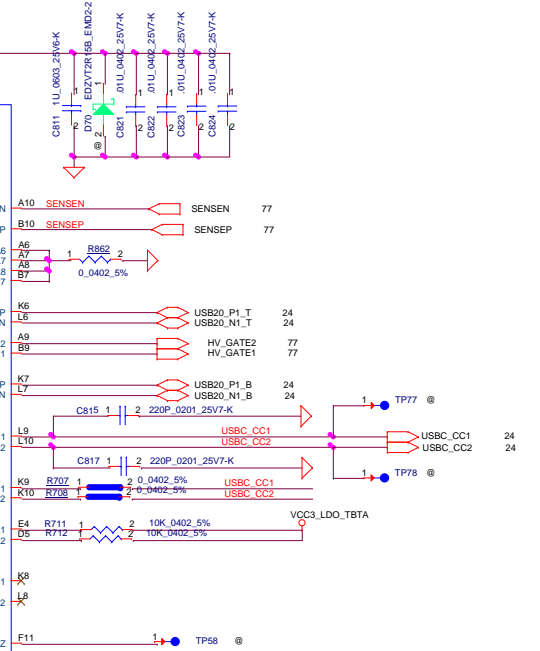
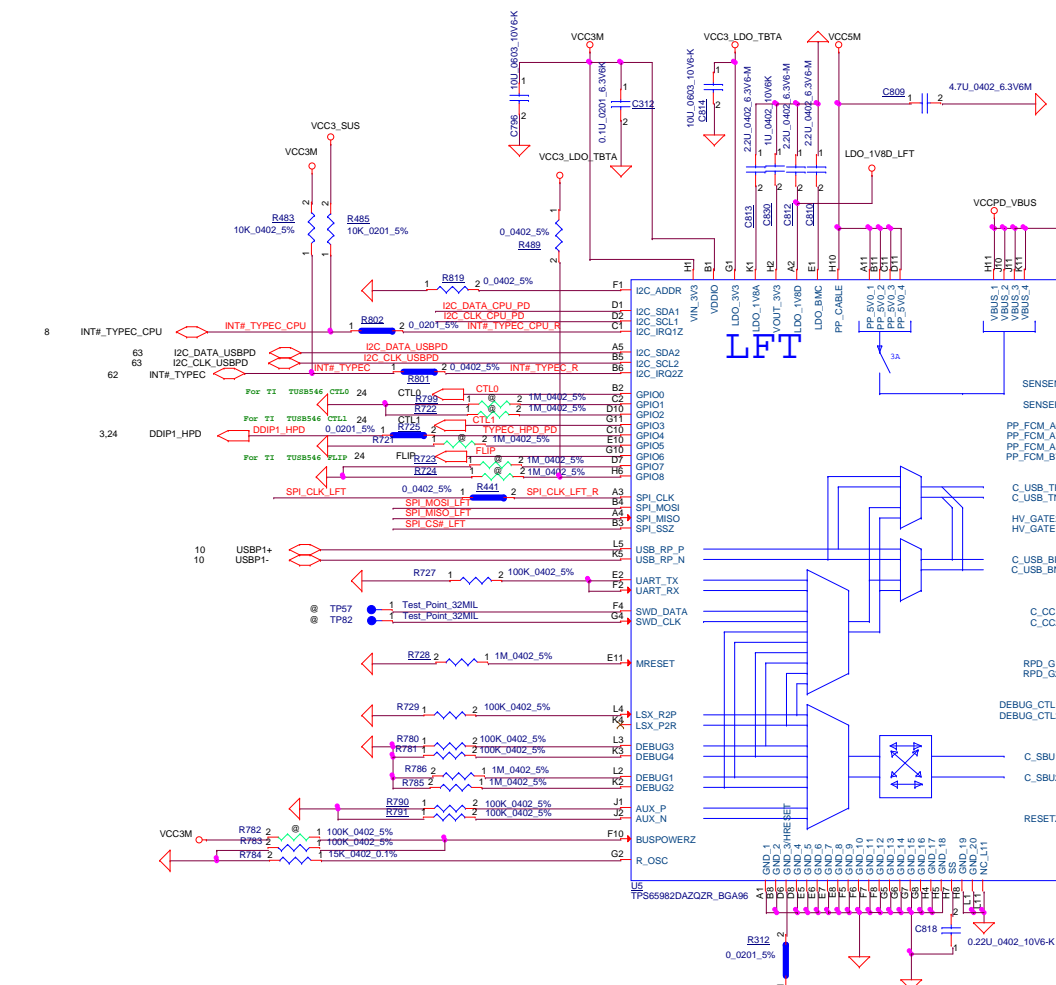
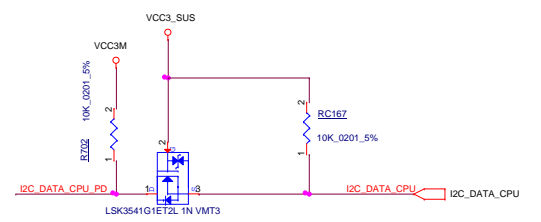
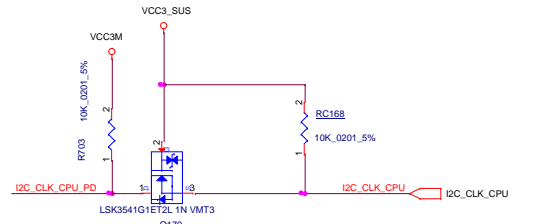
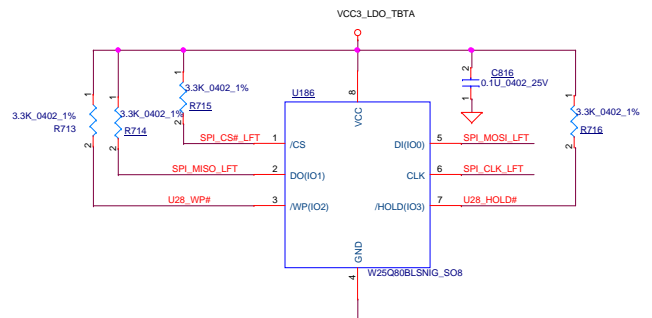



TABLE of SPI ROM (UC5)		
Vendor	MODEL	LCFC P/N
WINBOND	W25Q128JVSQ	SA00008A300
MXIC	MX25L12873FM2I-10	SA00005VM00

TABLE


SF100 PIN HEADER INTERFACE (TOP VIEW)					
1	VCC	DC4.1	GND	GND	2
3	CS#	RC128.2	GND	RC129.2	CLK
5	MISO	RC132.2	GND	RC130.2	MOSI
7	(KEY)	N/A	N/A	(RESET)	8




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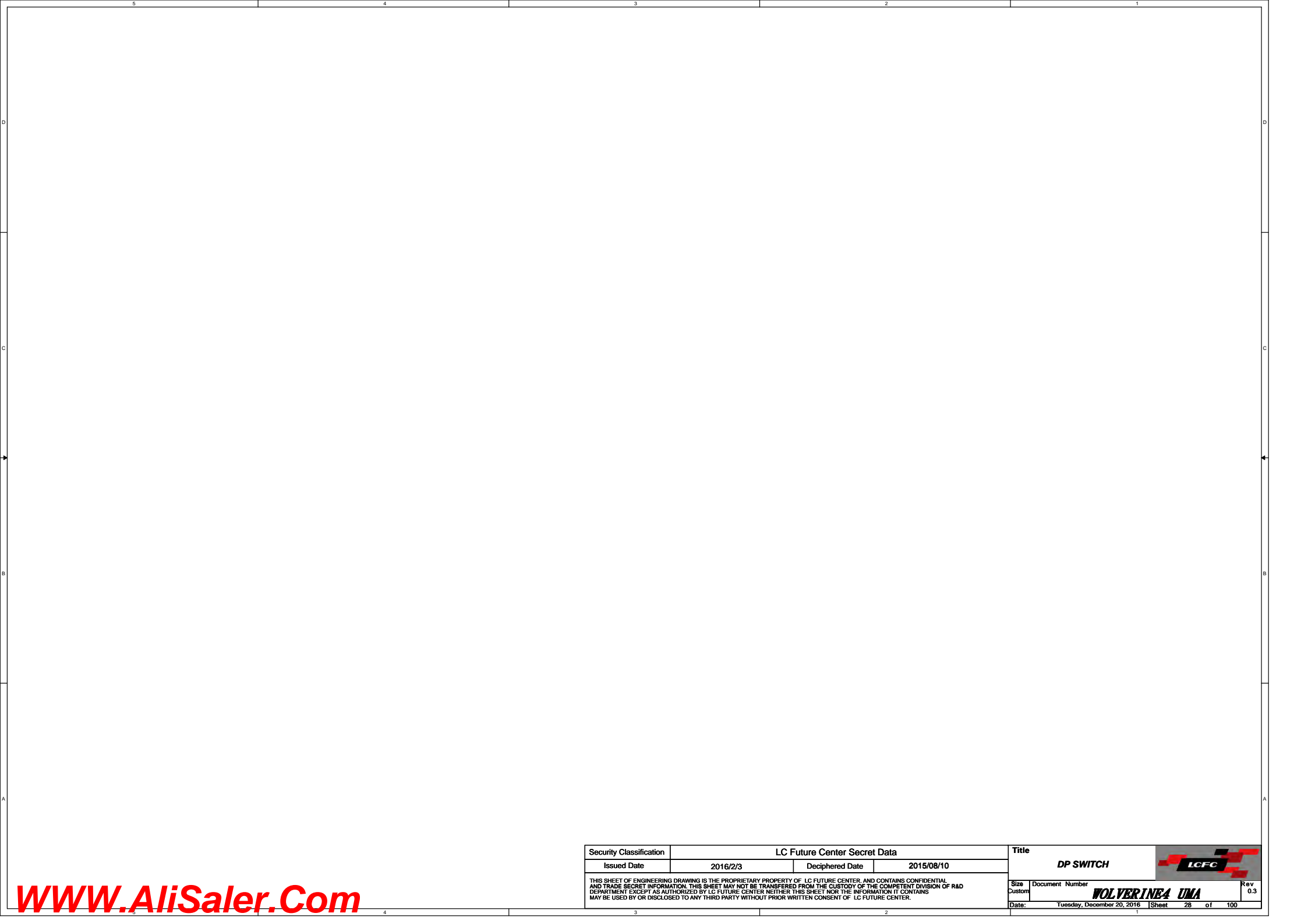
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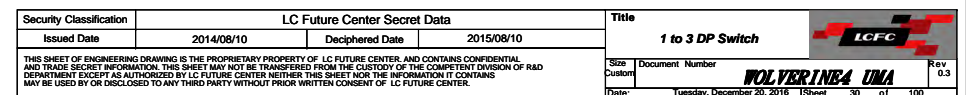
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Issued Date	2016/2/3	Deciphered Date	2015/08/10	DP SWITCH			
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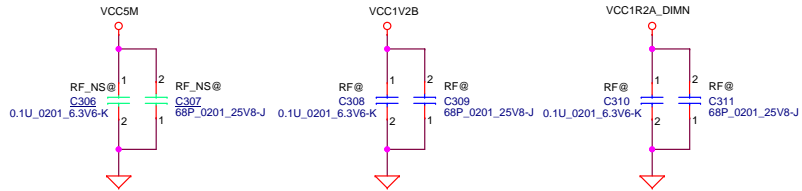
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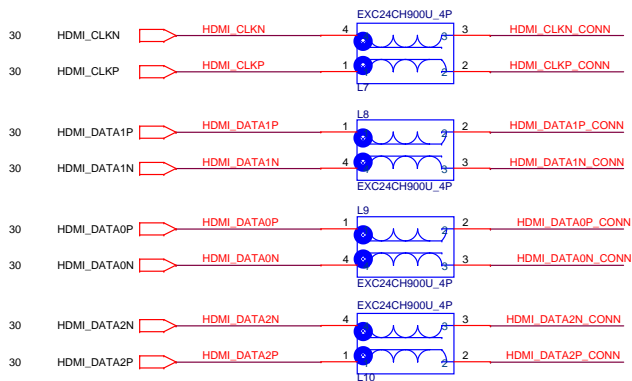
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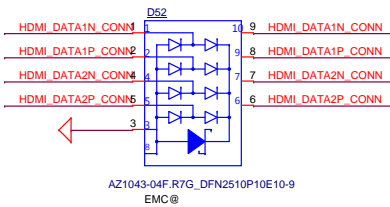
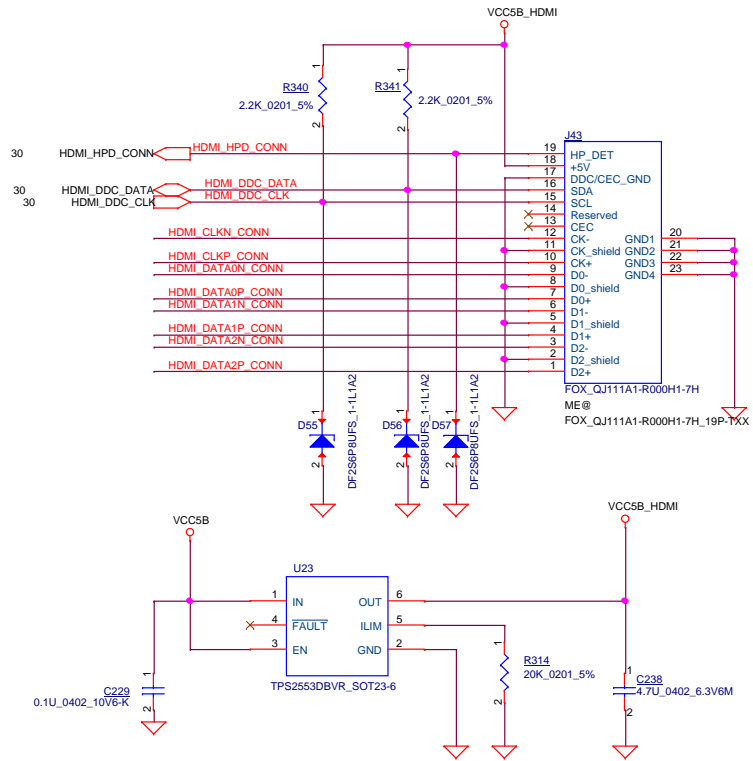
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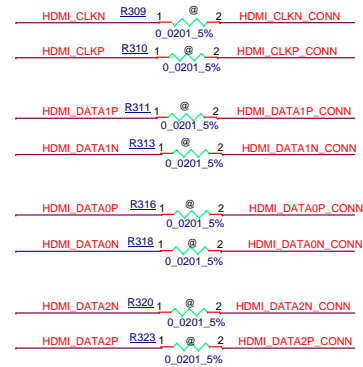
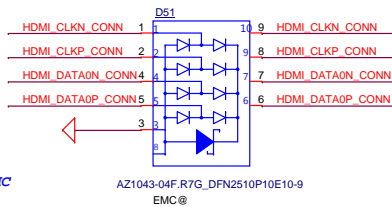


For PARADE Debug use.

HDMI_CLKN_CONN	R9121	1	2	180_0402_1%	HDMI_CLKP_CONN
HDMI_DATA1N_CONN	R9123	1	2	180_0402_1%	HDMI_DATA1P_CONN
HDMI_DATA0N_CONN	R9125	1	2	180_0402_1%	HDMI_DATA0P_CONN
HDMI_DATA2N_CONN	R9127	1	2	180_0402_1%	HDMI_DATA2P_CONN




For EMC




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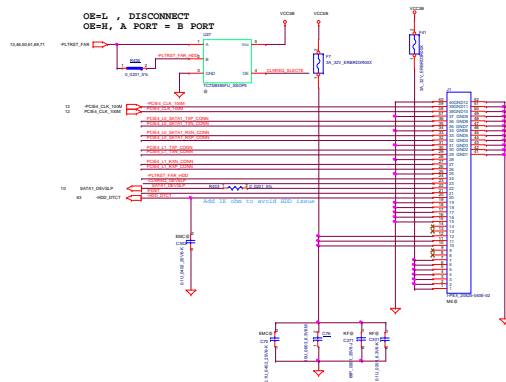
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Date:		Tuesday, December 20, 2016		Sheet 40 of 100	

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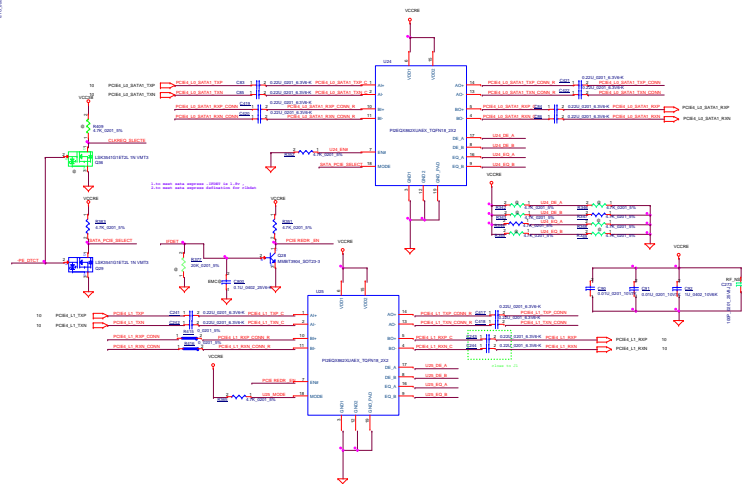
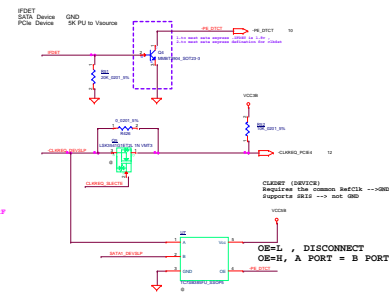
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30 E3 CLASSDET
 29 E2 REFCLON
 28 E1 REFCLAP
 27 S11 GND
 26 S12 PETAQA+
 25 S13 PETAQA-
 24 S14 GND
 23 S15 PERPUB+
 22 S16 PERPUB-
 21 S17 GND
 20 S18 GND
 19 S19 PETAH+
 18 S20 PETAH-
 17 S21 GND
 16 S22 PERST1
 15 S23 PERSTV
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 13 S25 CLASSDET
 12 P3 CLASSDET
 11 P2 GND
 10 P1 GND



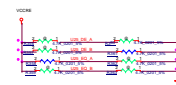
Mode Configuration Table		
ENR	MODE	MODE
0	0	SATA Application
0	1	PCIe Application
1	0	Disable

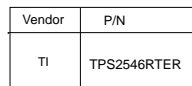
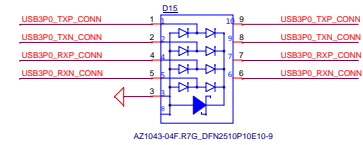
Equalization Setting:
EQ1, EQ2 are the selection pins for the equalization selection for each direction.

Equalizer setting		
EQ1, EQ2	EQ1EQ2	EQ1EQ2
0	00	00
0	01	01
1	10	10
1	11	11

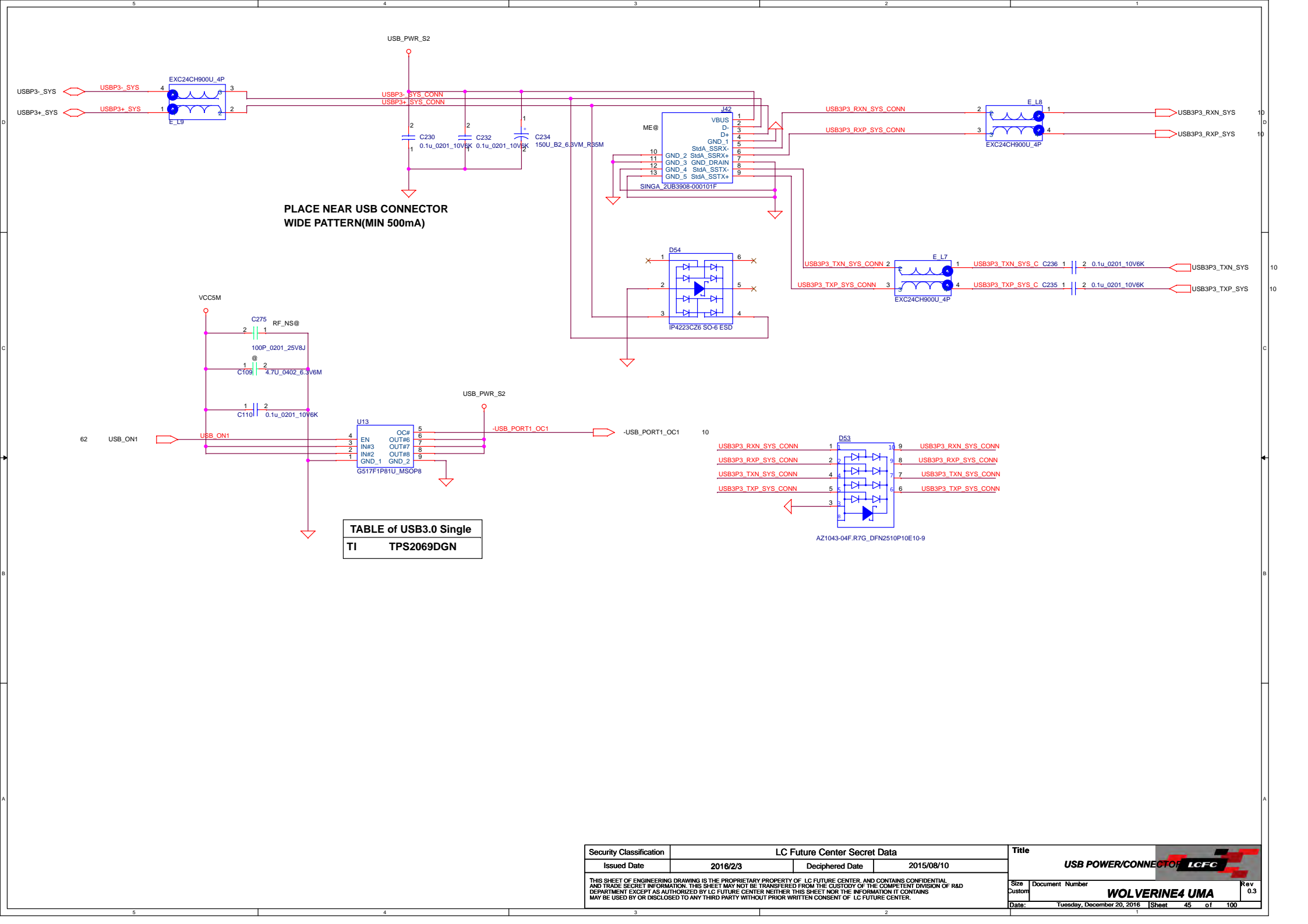
De-emphasis Setting (for PCIe only):

Output DE-emphasis Setting		
DE	DE	DE
0	0	0
0	1	1
1	0	0
1	1	1





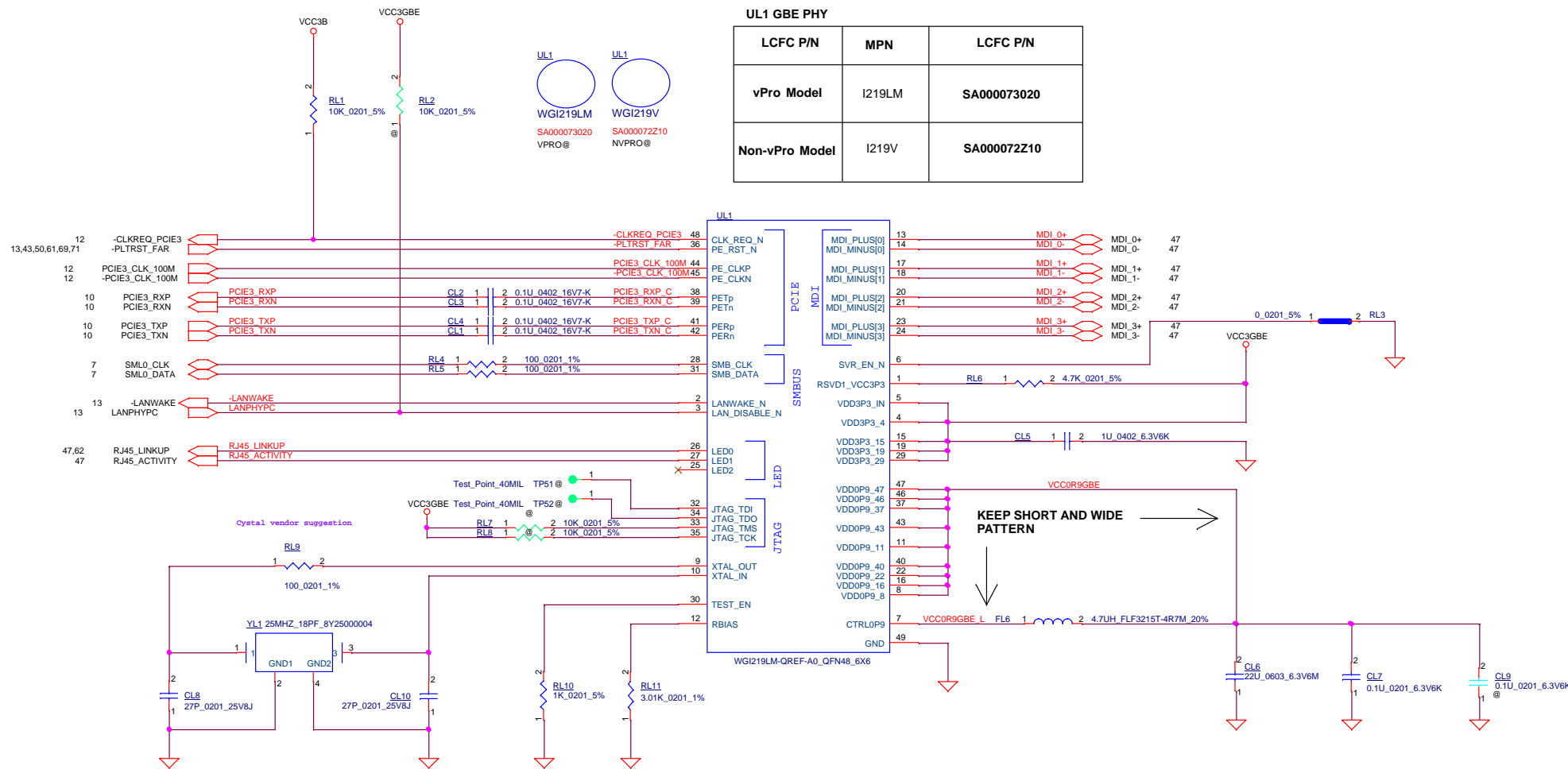
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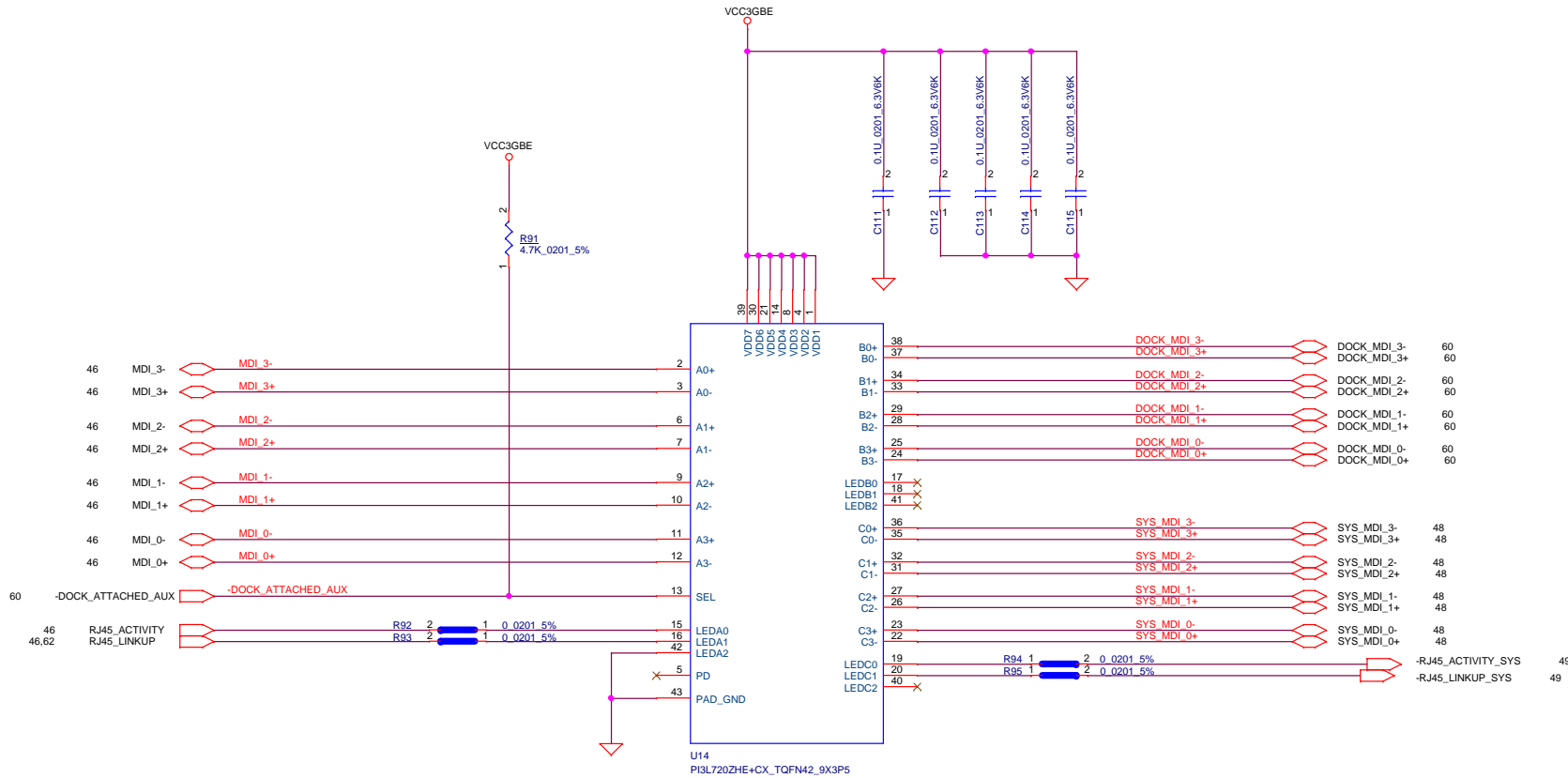
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Title		Rev	
USB POWER/CONNECTOR		0.3	
Size	Document Number	WOLVERINE4 UMA	
Custom			
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YL1 25Mhz

Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
TXC	50 ohm Max	SJ10000H00J	8Y25000004	50 ohm Max
KDS	50 ohm Max	SJ10000P300	1ZZHAE25000CC0F	50 ohm Max



U14 GBE LAN SWITCH TABLE

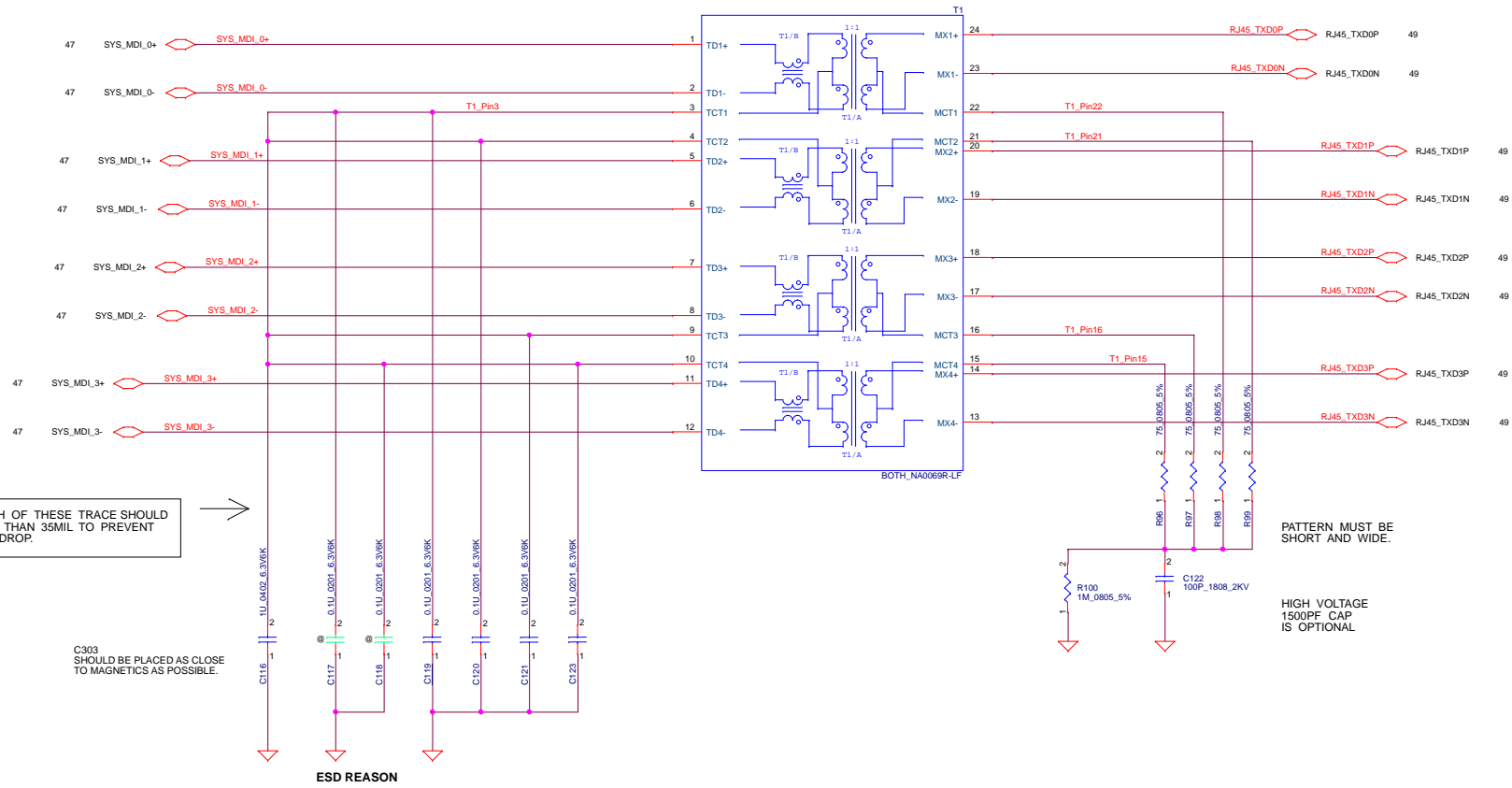
LCFC P/N	VENDOR	MPN
SA00007E900	PERICOM	PI3L720ZHE+CX
SA000072400	TI	TS3L501ERUAR

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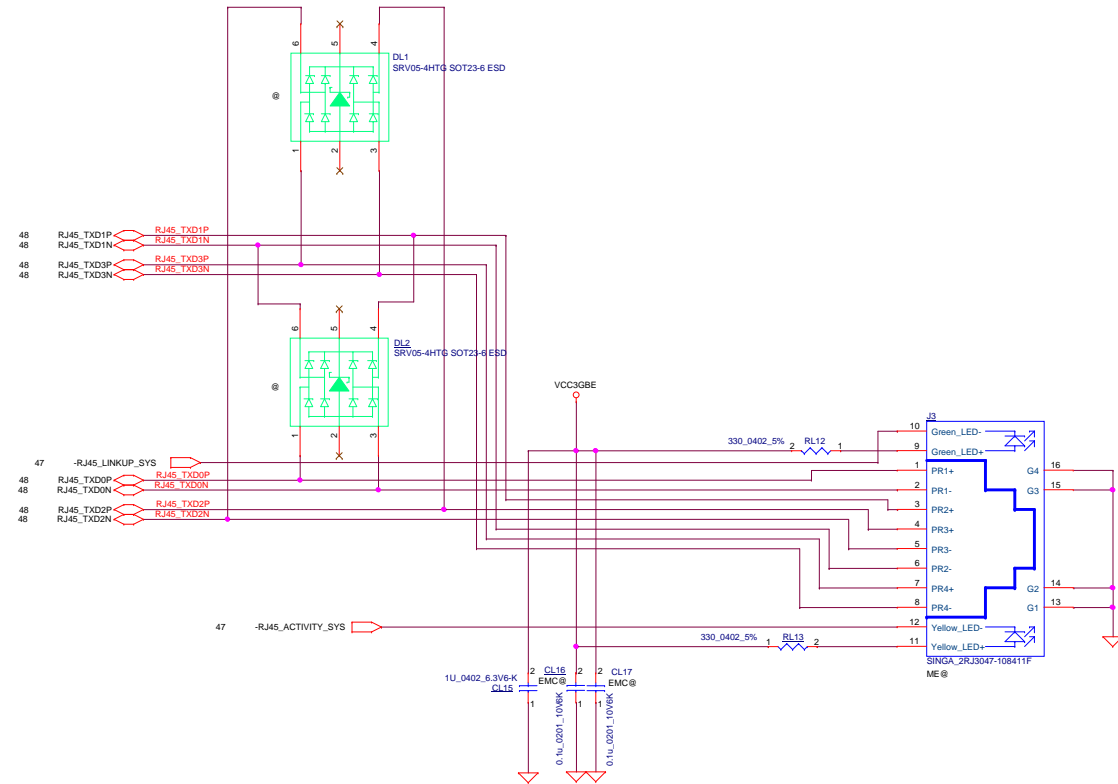
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Size	Document Number	Rev	
Custom		0.3	
Date:	Tuesday, December 20, 2016	Sheet	47 of 100



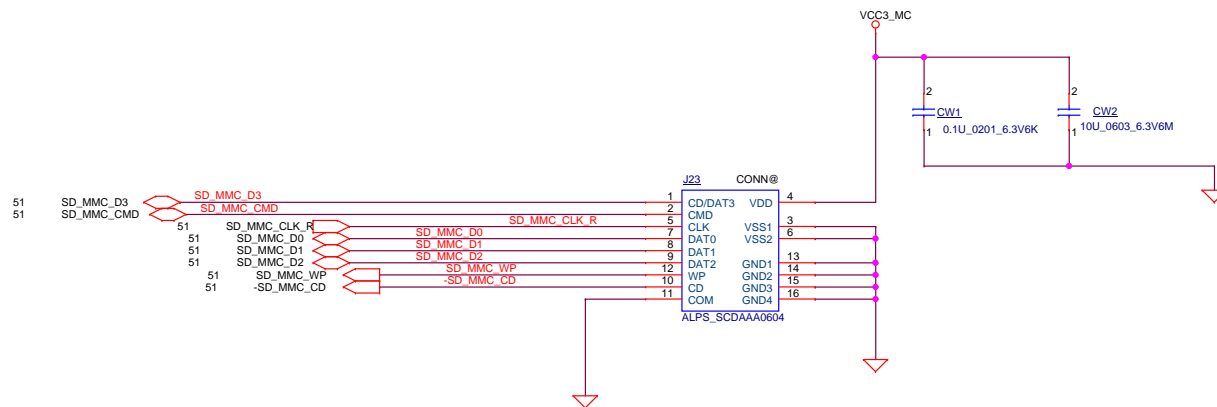
VOLVERINE4 UMA



Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF



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Custom	VOLVERINE4		UMA		
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Size	Document Number	Rev			
Cuslon		WOLVERINE4 UMA			0.3
Date:		Tuesday, December 30, 2016		Sheet 53 of 100	

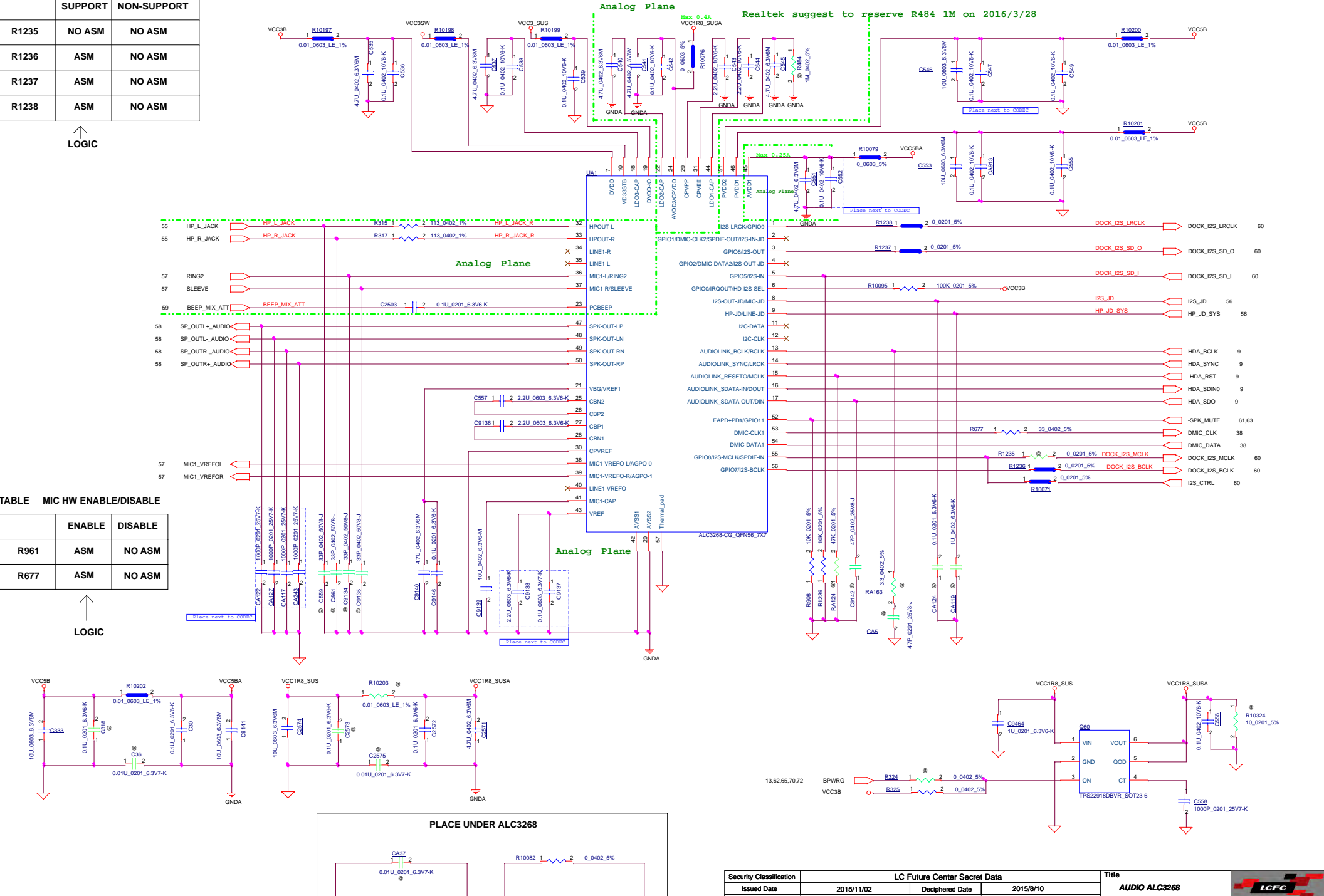
TABLE		
Dock support		
	SUPPORT	NON-SUPPORT
R1235	NO ASM	NO ASM
R1236	ASM	NO ASM
R1237	ASM	NO ASM
R1238	ASM	NO ASM


↑
LOGIC

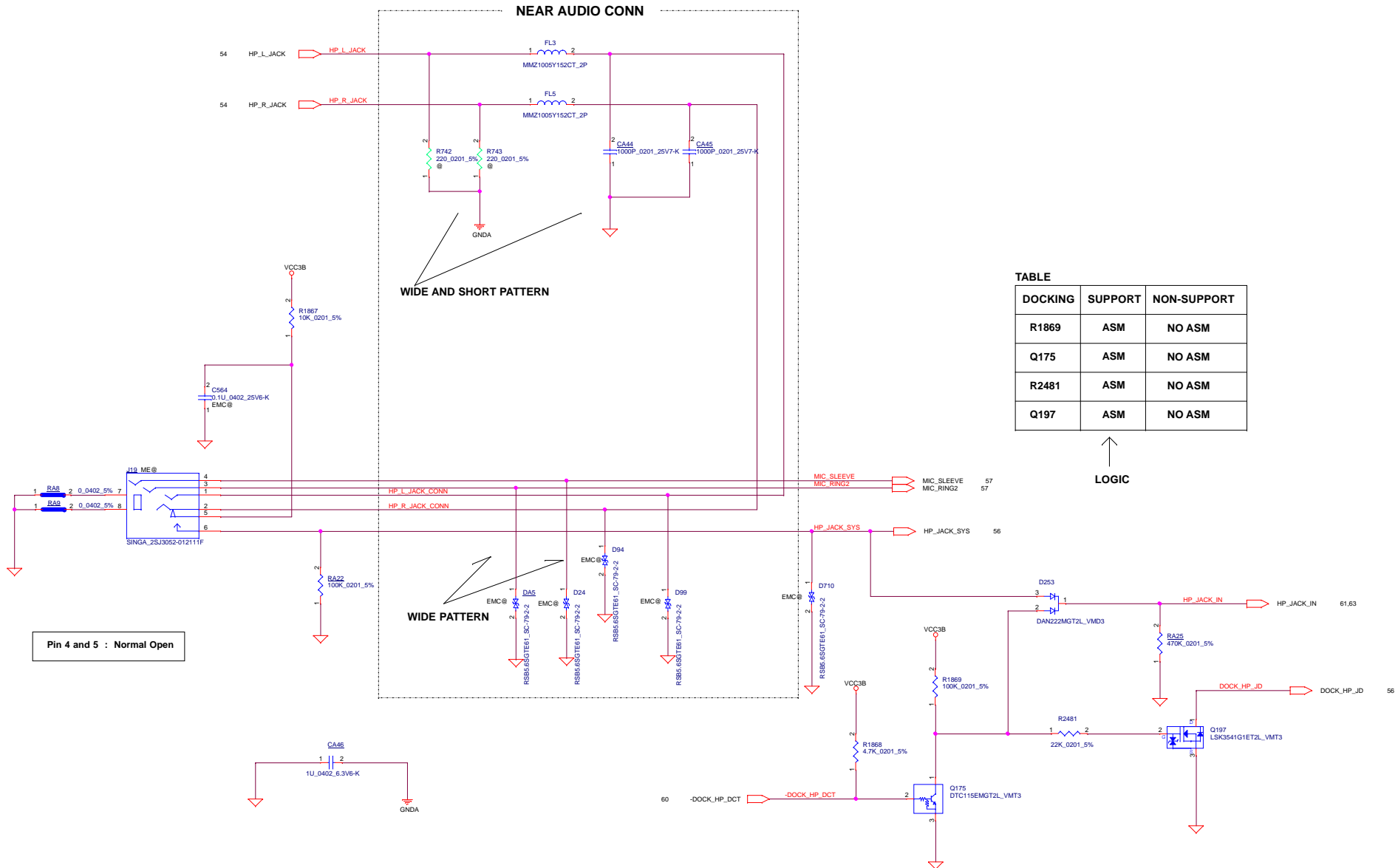
TABLE MIC HW ENABLE/DISABLE

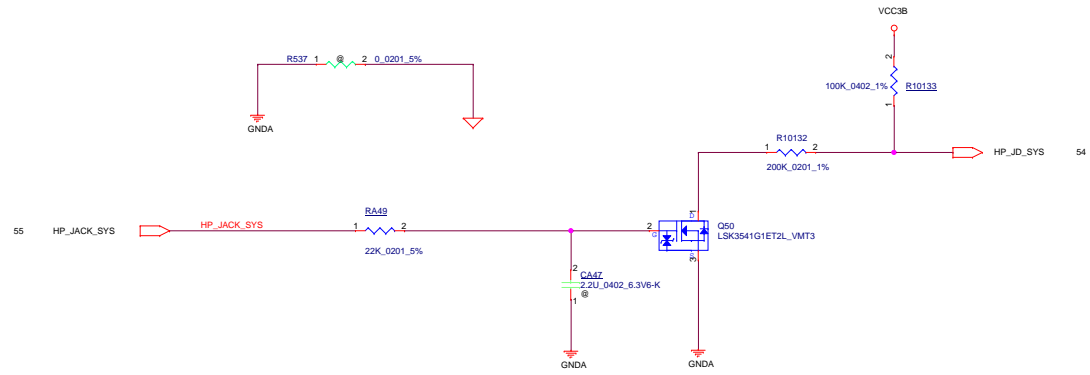
	ENABLE	DISABLE
R961	ASM	NO ASM
R677	ASM	NO ASM

↑
LOGIC



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Size	Document Number	Date		 WOLVERINE4 UMA Rev 0.3 Tuesday, December 20, 2016 15:54:01	

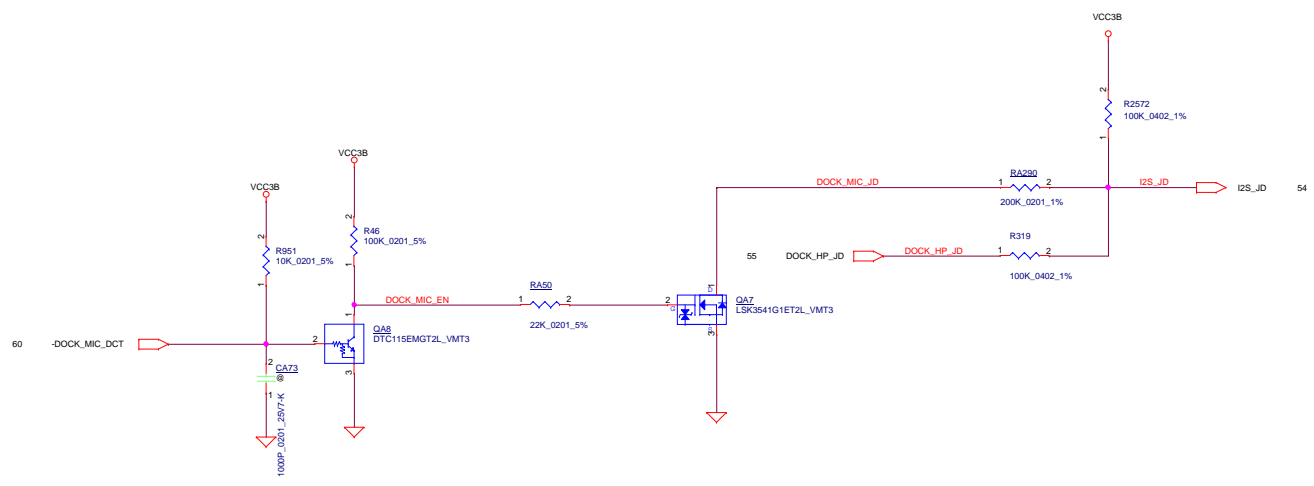


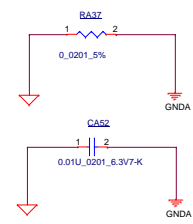
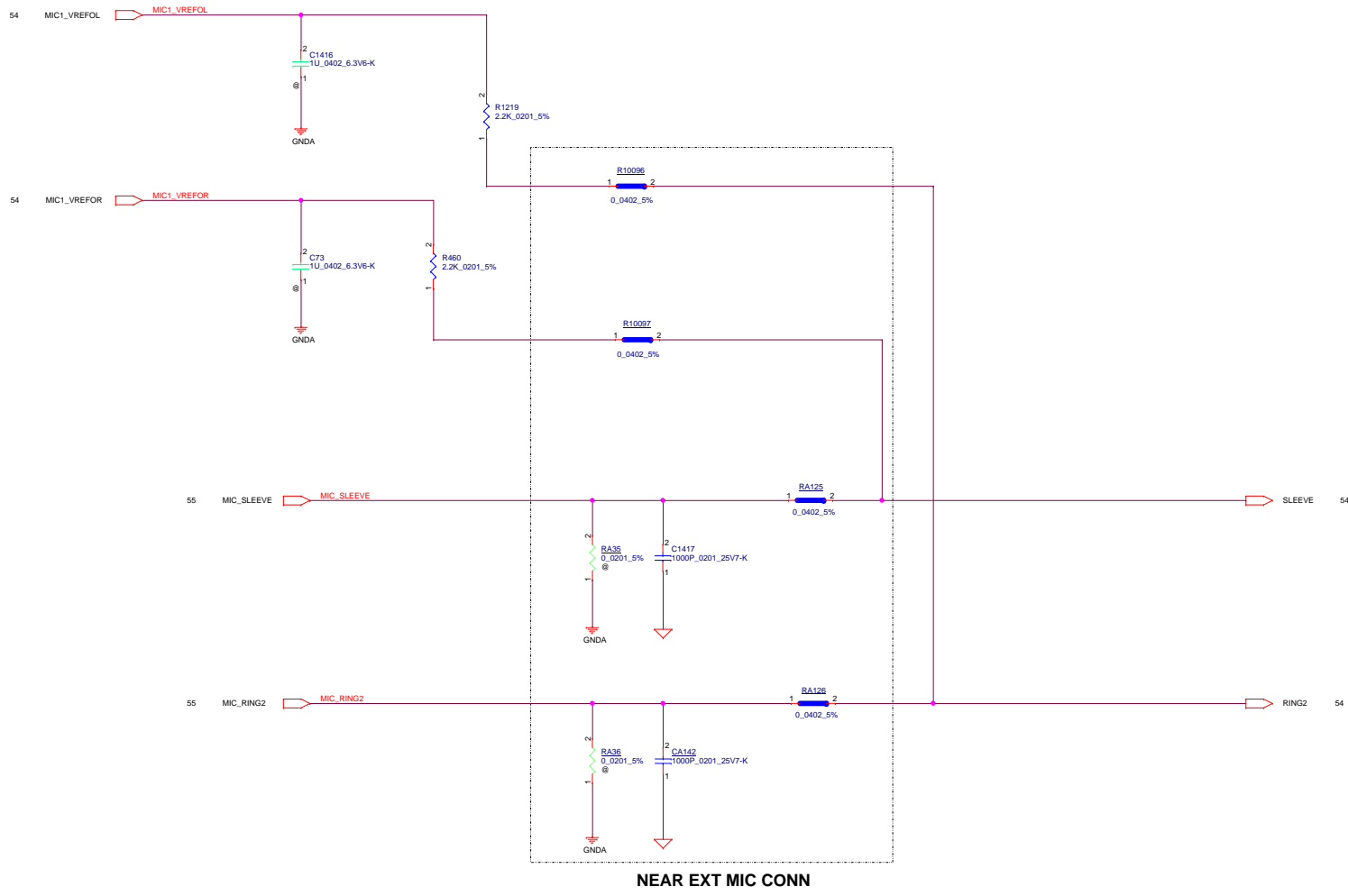


TABLE

DOCKING	SUPPORT		NON SUPPORT
	ENABLE	DISABLE	
R951	ASM	NO ASM	NO ASM
R290	ASM	NO ASM	NO ASM
R46	ASM	NO ASM	NO ASM
Q5	ASM	NO ASM	NO ASM
R52	ASM	NO ASM	NO ASM
Q6	ASM	NO ASM	NO ASM
R319	ASM	ASM	NO ASM
R2572	ASM	ASM	NO ASM

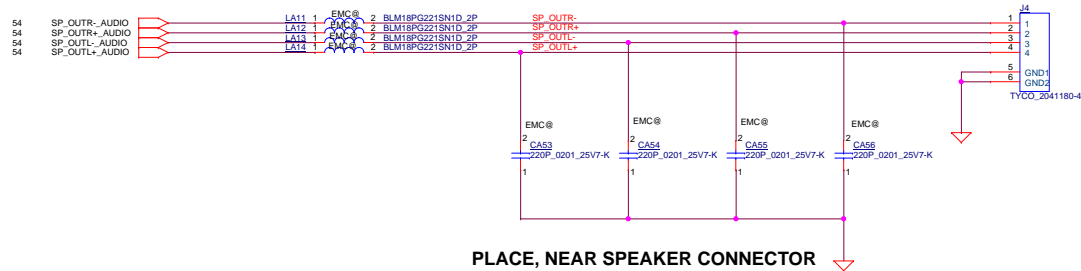
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LOGIC




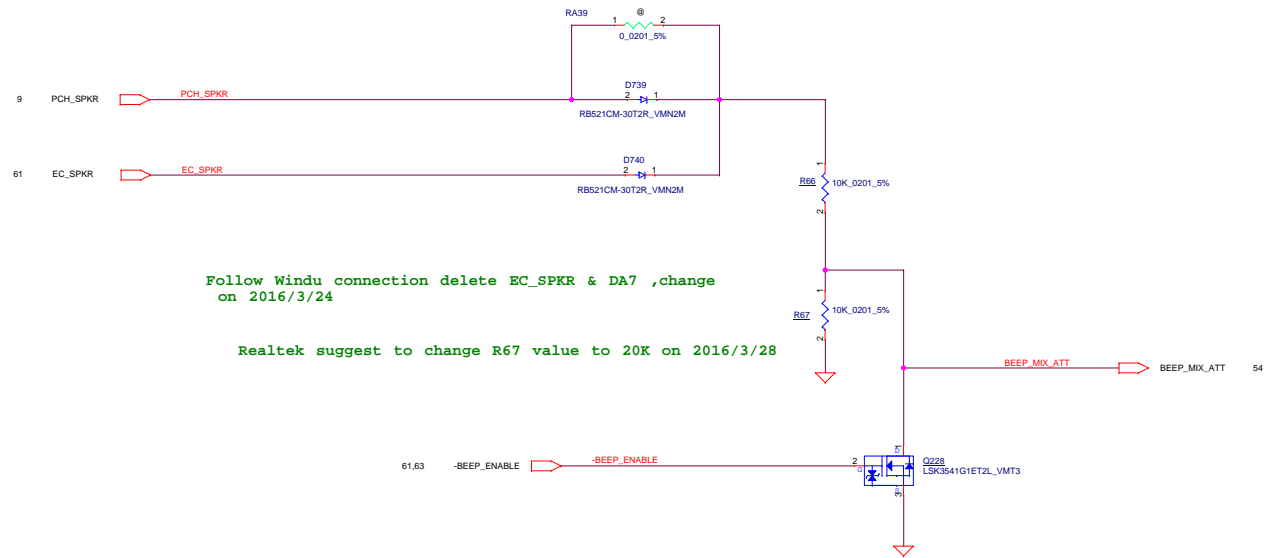


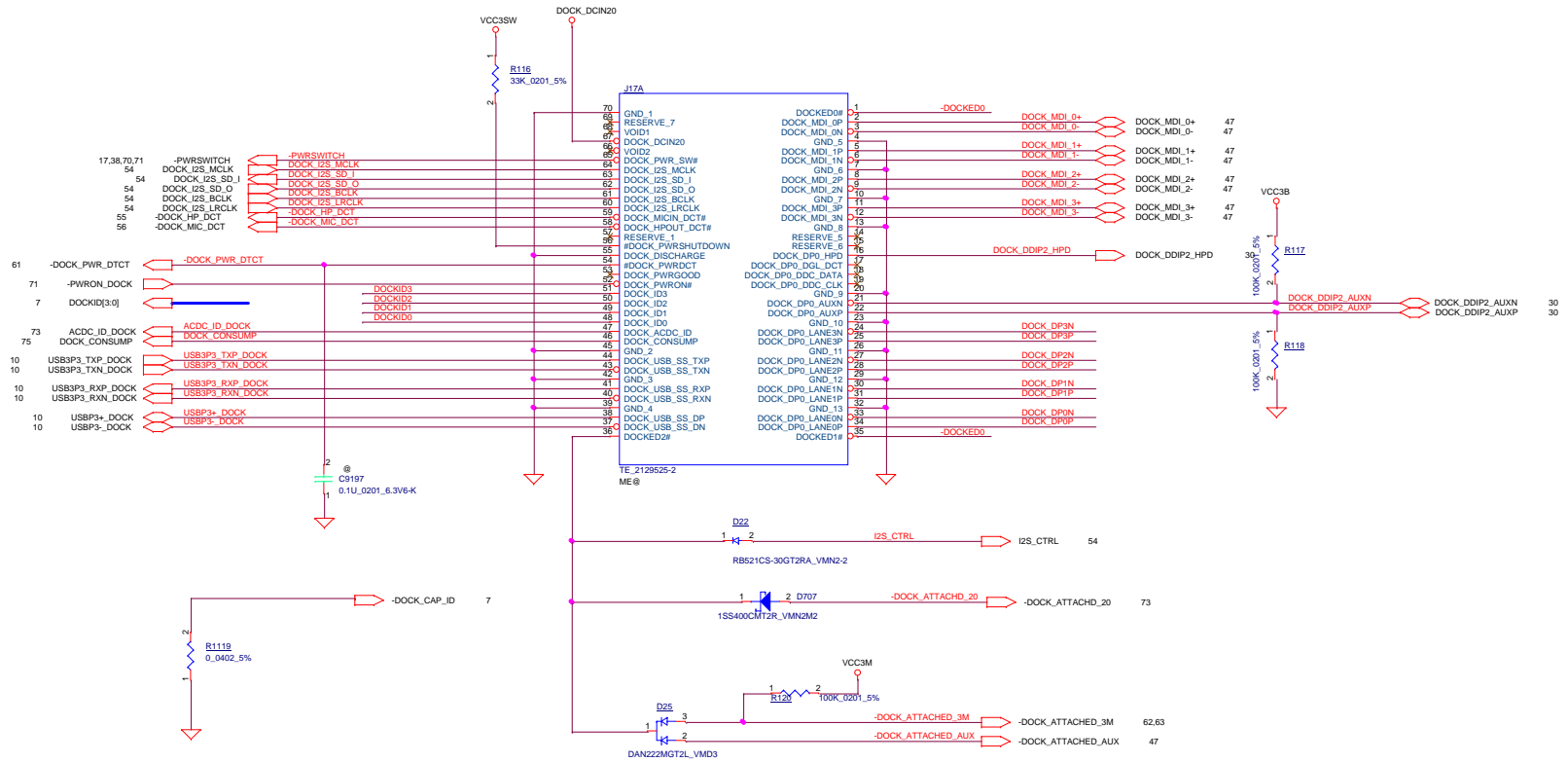
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Issued Date	2015/11/02	Deciphered Date	2015/8/10	AUDIO EXT MIC I/F	
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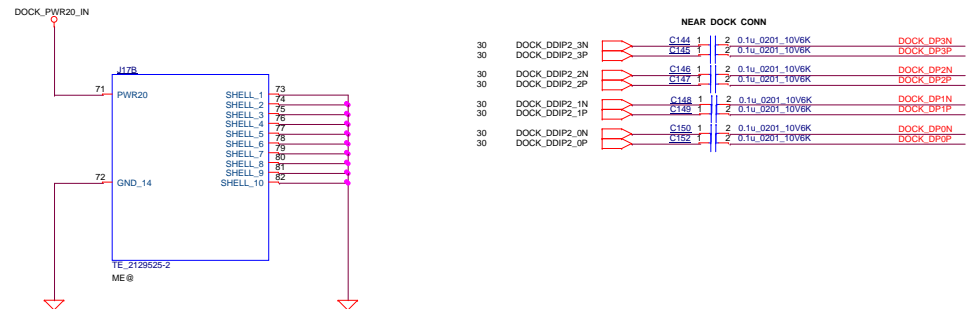
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Issued Date		2015/11/02		Deciphered Date		2015/8/10		AUDIO SPEAKER		
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Custom		C						0.3		
Date:		Tuesday, December 30, 2016		Sheet		59		61		100




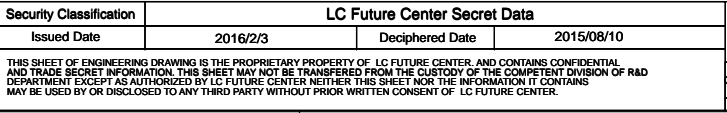


20160222 change to reserved to avoid duplicated DOCK_PWR20_IN

Q6 & D23 delete on 2016/3/17, DOCK_PWR20_IN power rail provided form PWR page



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Issued Date		Deciphered Date		DOCKING CONNECTOR	
2016/2/3		2014/08/10			
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Customer		VOLVERINE 4		0.3	
Date:		Tuesday, December 30, 2016		Sheet	
				50 of 100	



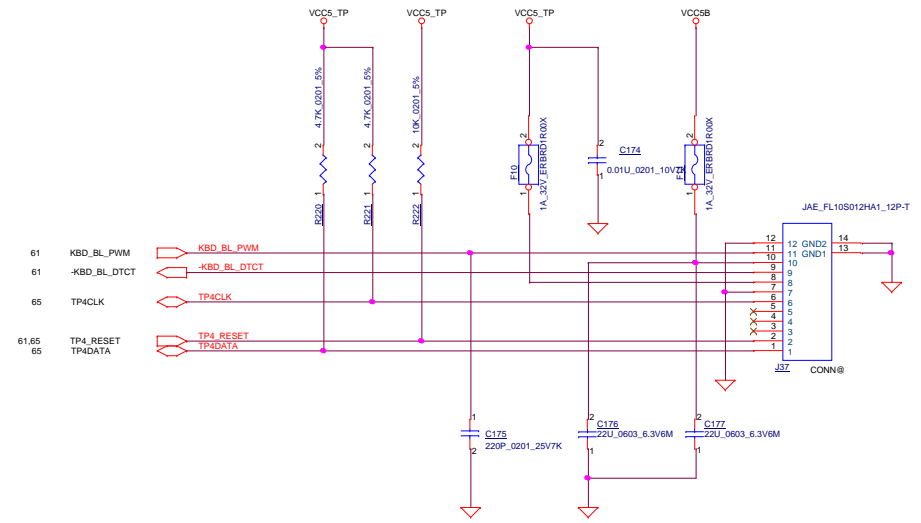
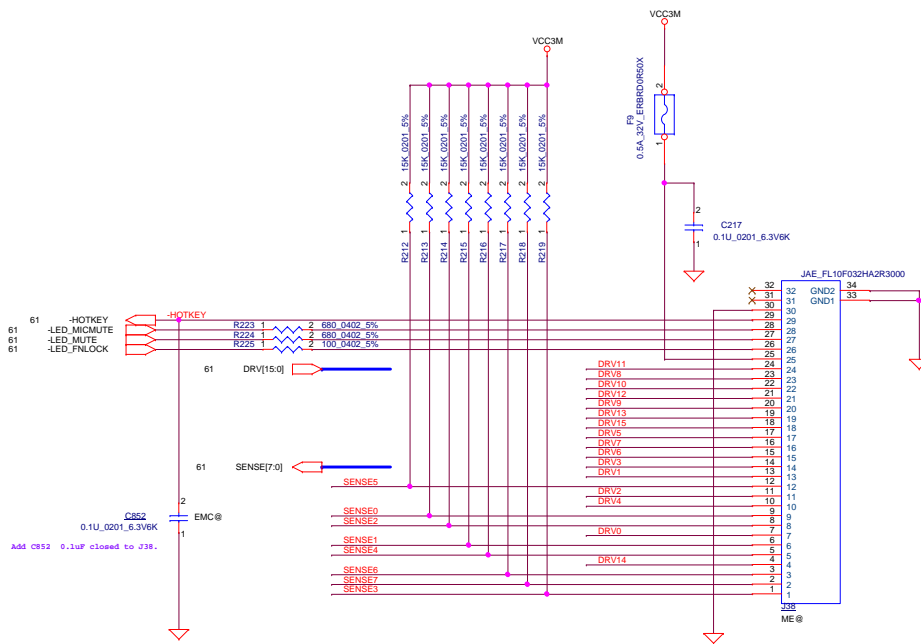


Sensor	Device	Placed on
C161+Q9	CPU DC/DC(PU402)	BOTTOM
C164+Q11	DIMM (J21)	BOTTOM
C167+Q13	WLAN (J32)	BOTTOM
C255+Q25	FAN module	TOP
C163+Q10	Charger (PU101)	BOTTOM
C166+Q12	WWAN(J22)	BOTTOM

JTAG Pin Connection

JTAG Pin Number	Net Name
Pin1	-DOCK_ATTACHED_3M(TP11)
Pin2	BDC_ON(TP7)
Pin3	-WLAN_DISABLE(TP12)
Pin4	-WLAN_RF_KILL(TP6)
Pin5	GND
Pin6	VCC3M
Pin7	GND
Pin8	GND

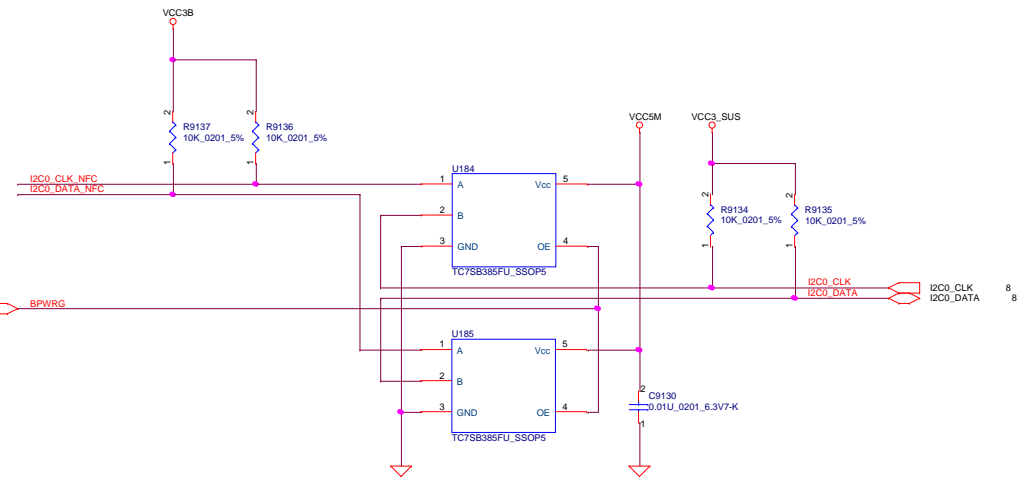
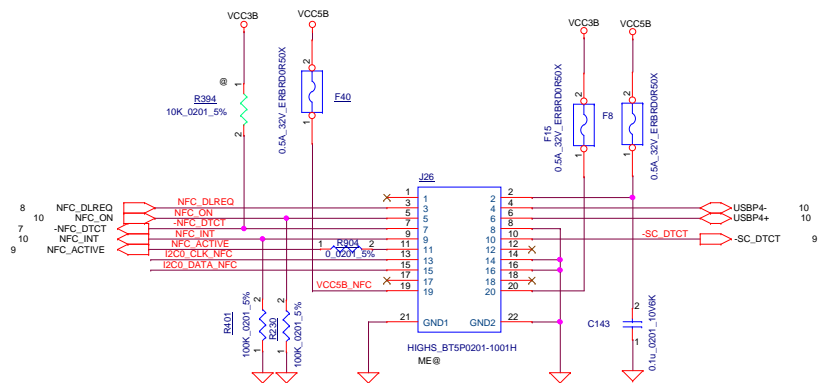
JTAG Debug Port	Enable	Disable
R181	ASM	NO ASM
R182	NO ASM	ASM
R206	ASM	NO ASM
R209	ASM	NO ASM
R210	NO ASM	ASM
R211	ASM	NO ASM



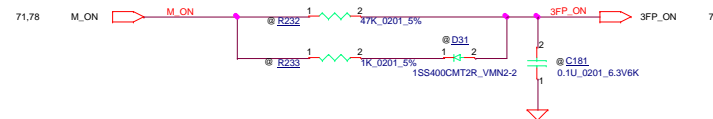
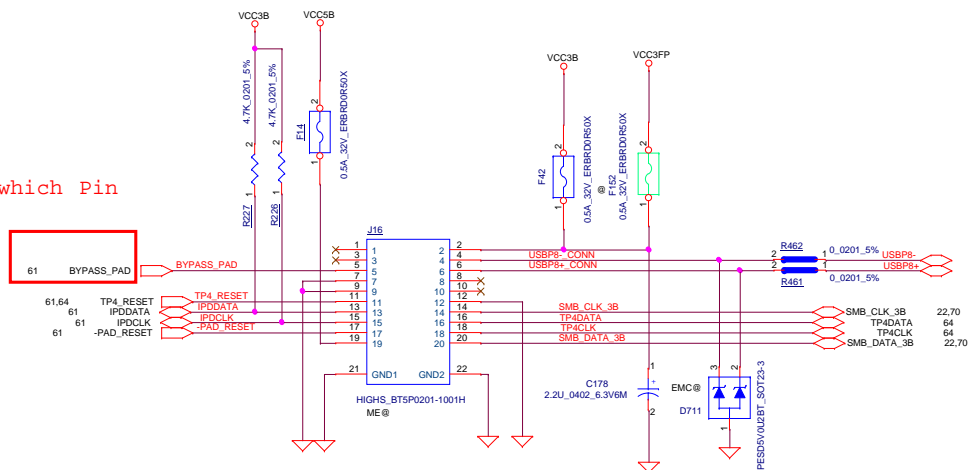
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Issued Date	2016/2/3	Deciphered Date	2015/08/10	KEYBOARD/TRACK POINT	
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0.3

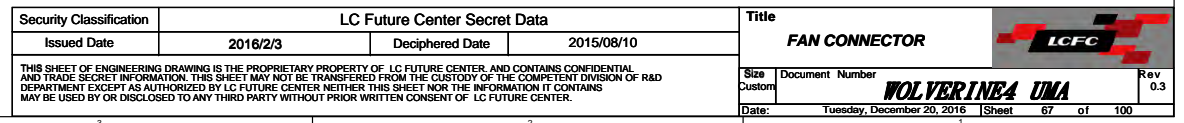


Check which Pin



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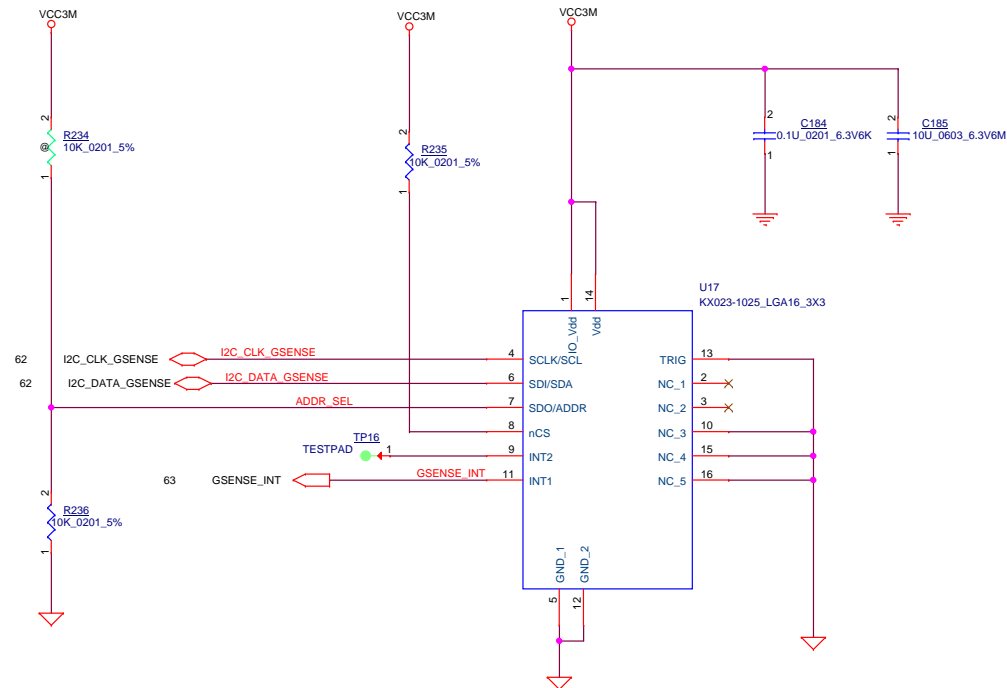
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			Sheet	66 of 100



G-SENSOR TABLE

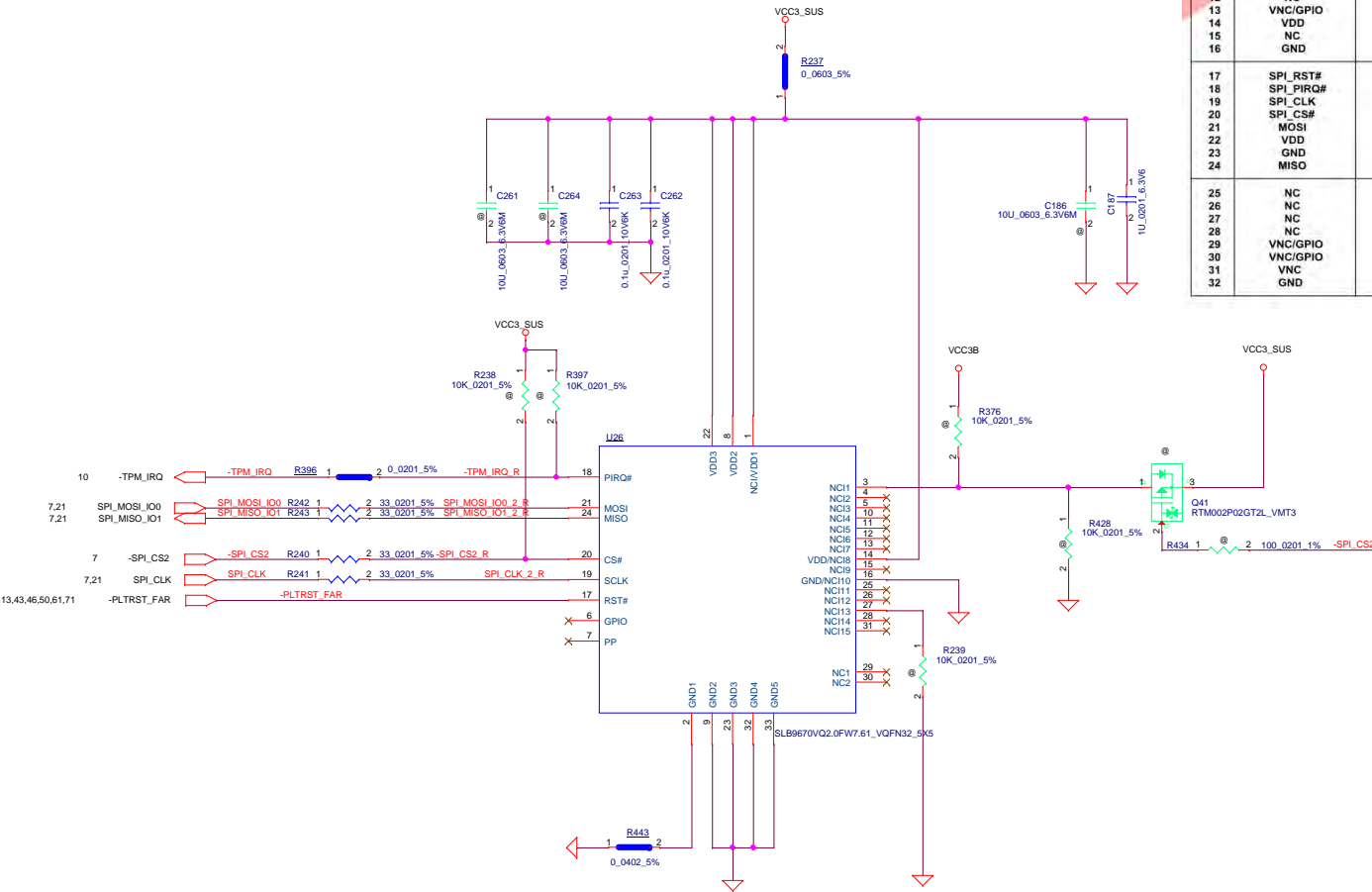
U17 PIN8 nCS	Mode Selection
H	I2C Mode
L	SPI Mode

LCFC P/N	ADDR_SEL	Address
LIS3DH SA00007Q700	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX023-1025 SA000073P00	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)



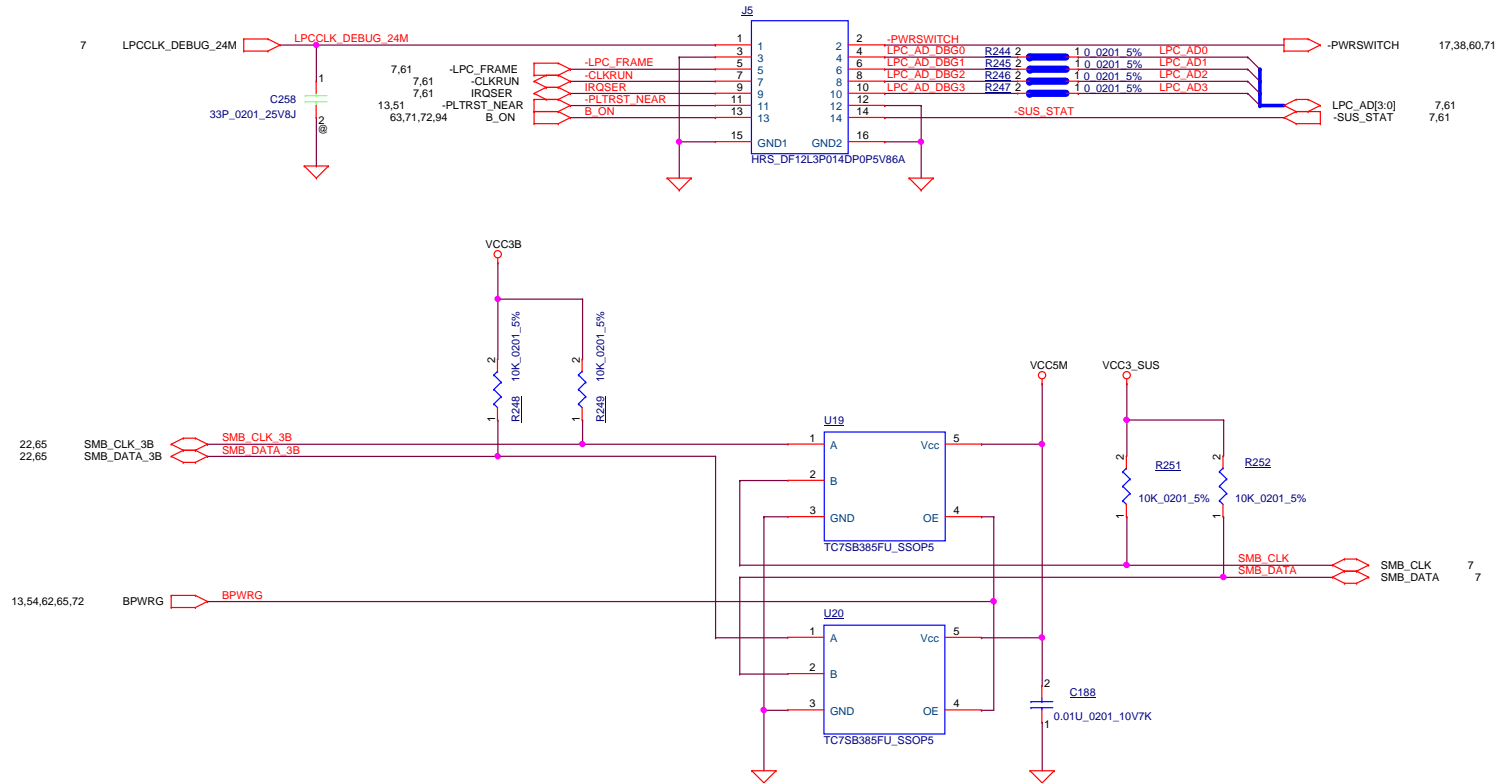
TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	NC	NC
3	GPIO	NC	NC	GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND



LPC Debug port TABLE

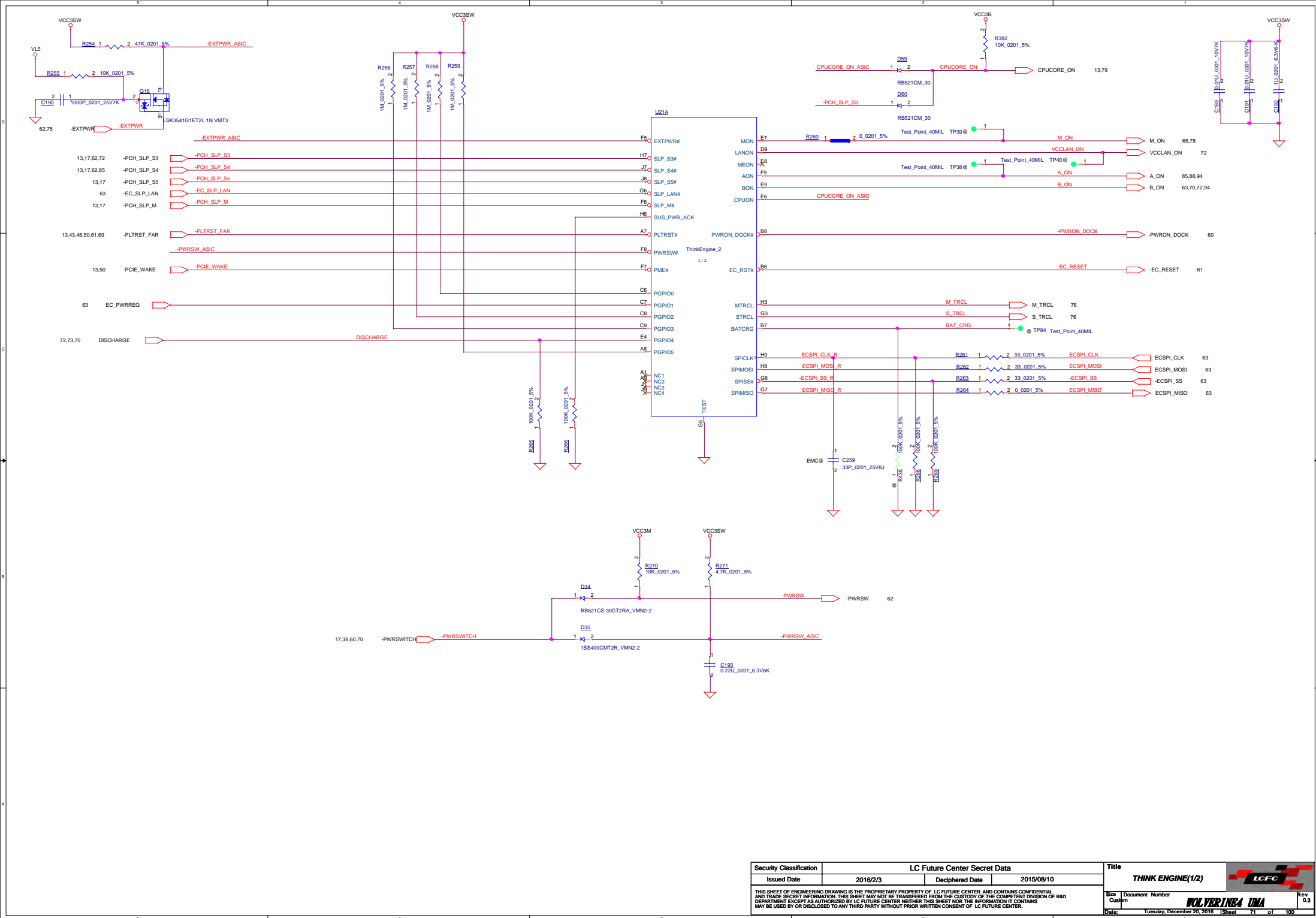
	Planner Only	BOX
J5	ASM	NO_ASM
RC29	ASM	ASM



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Title		LCFC	
SMBUS SW/LPC DEBUG PORT			
Size	Document Number	Rev	0.3
Custom			
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VOLVERINE4 UMA





DCIN



Total MLCC capacitance at DCIN connector is smaller than 1000pF to avoid LC resonance

DCIN_PWR

PLACE NEAR CONNECTOR DCIN_PWR20_F

DCIN_PWR20_F

DOCK_PWR20_IN

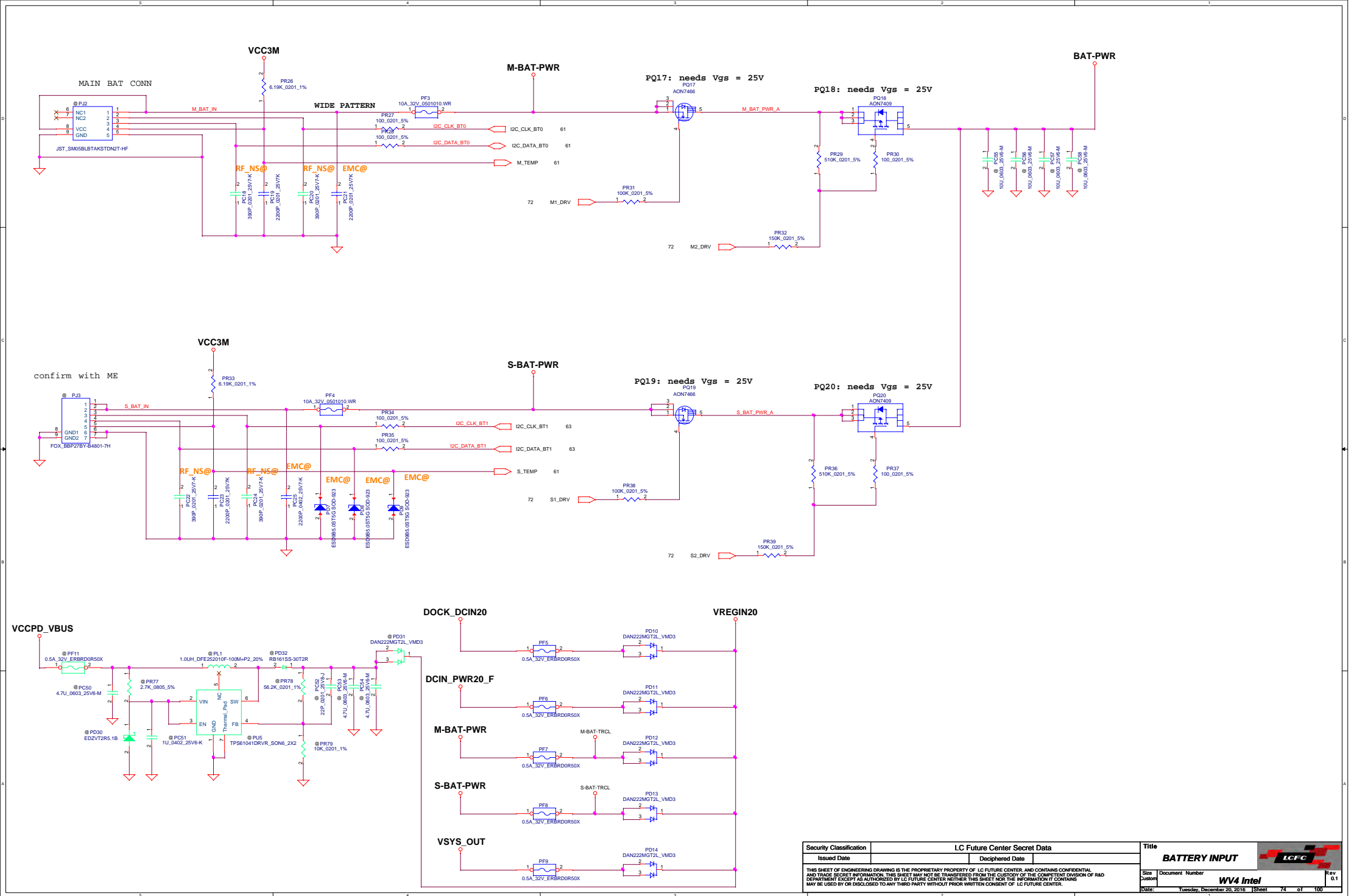
DOCK_ATTACHD_20

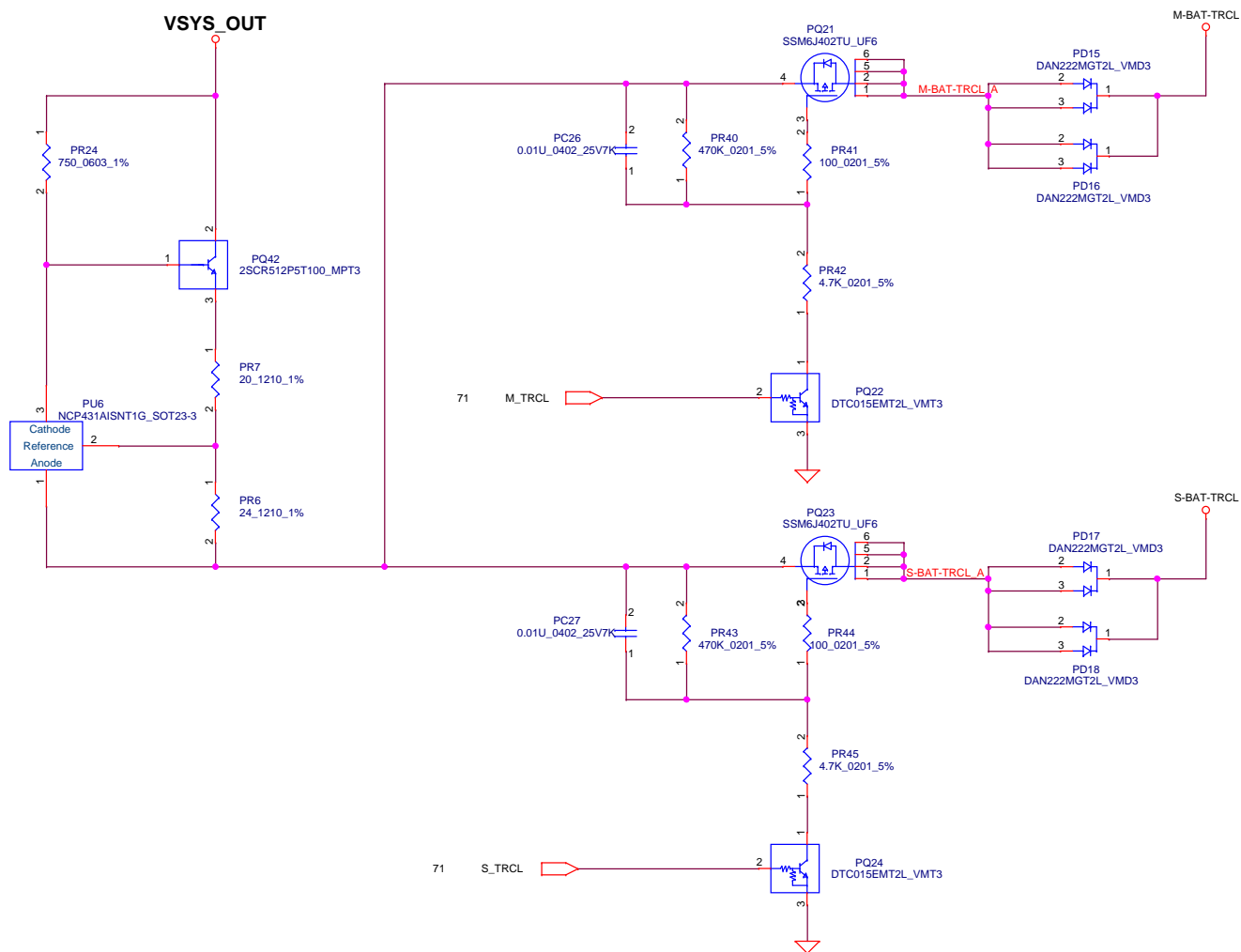
ADAPTER_ID_ON#


VINT20_IN

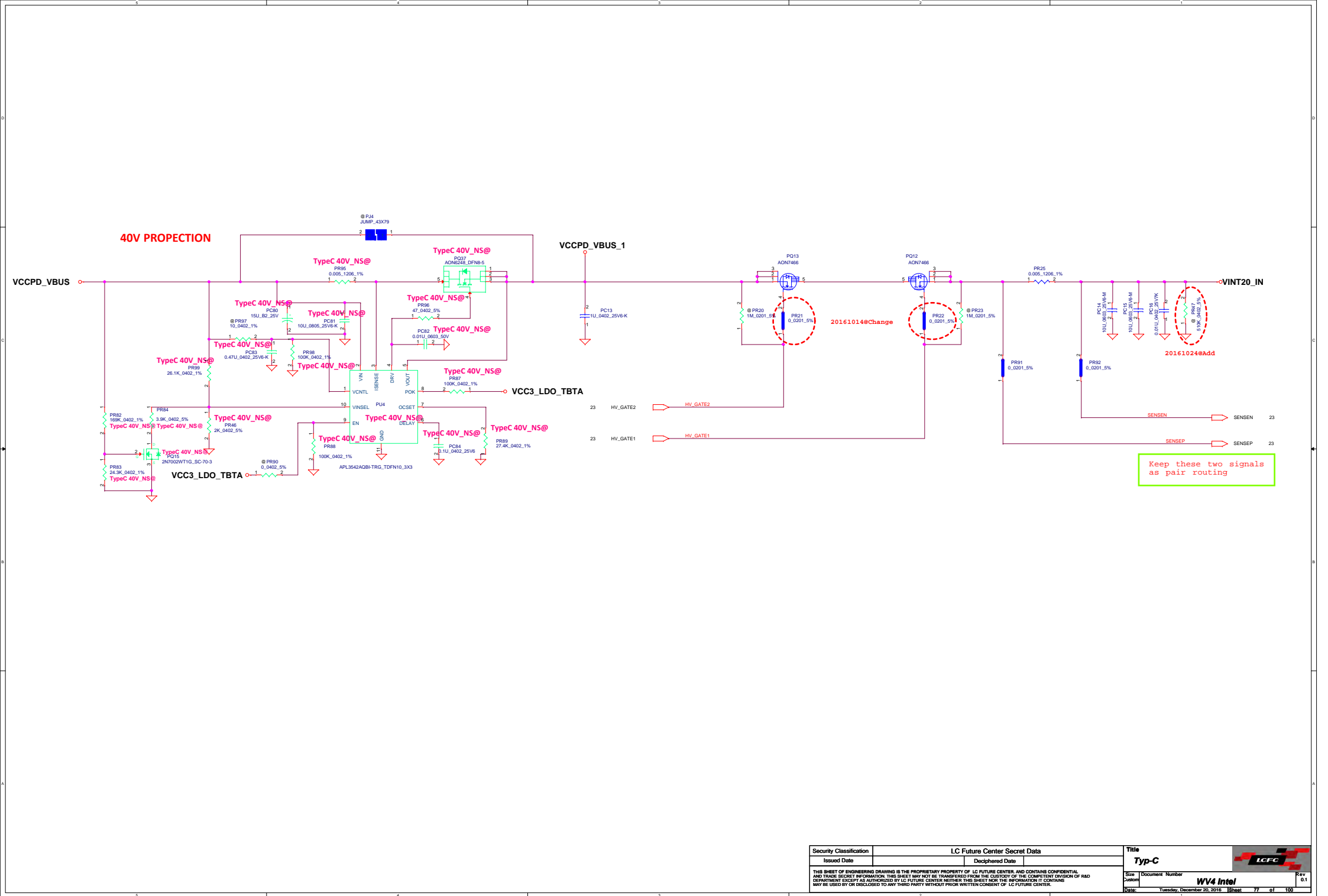
DISCHARGE

PWRSHUTDOWN





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			Document Number WV4 Intel	
			Date: Tuesday, December 20, 2016	Rev 0.24
			Sheet 76 of 100	

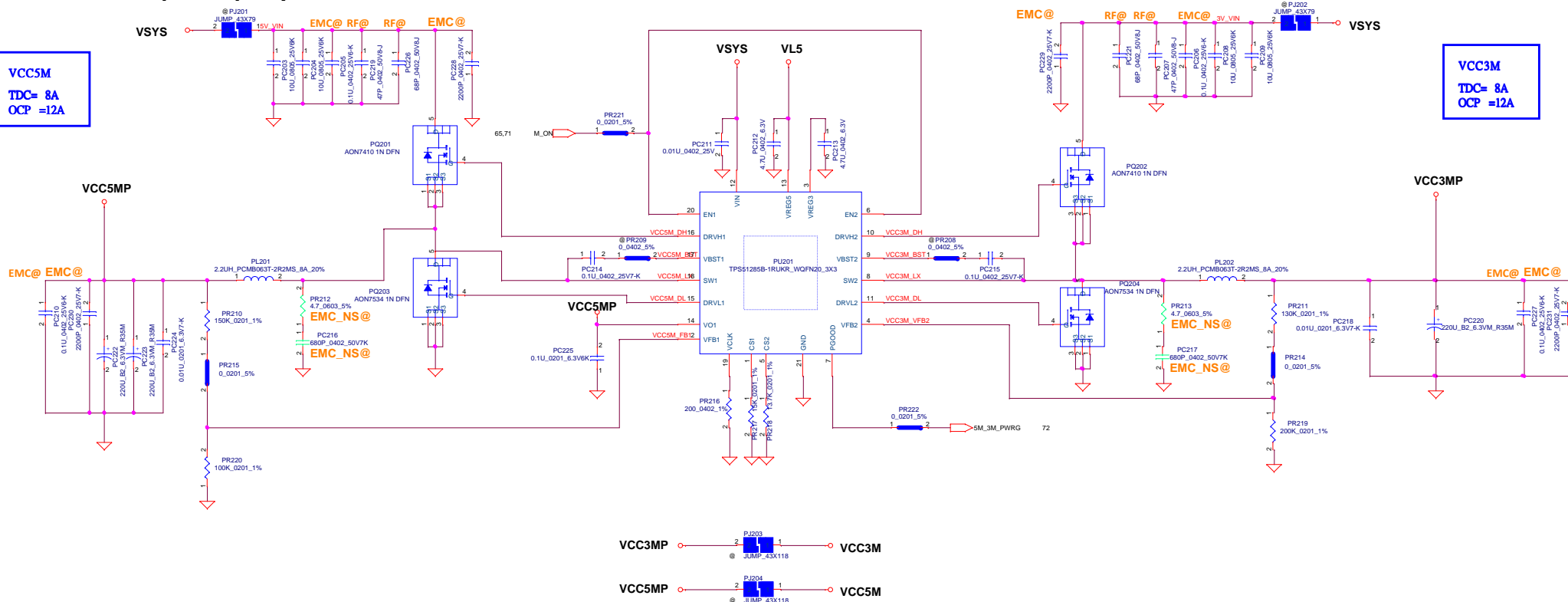


All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

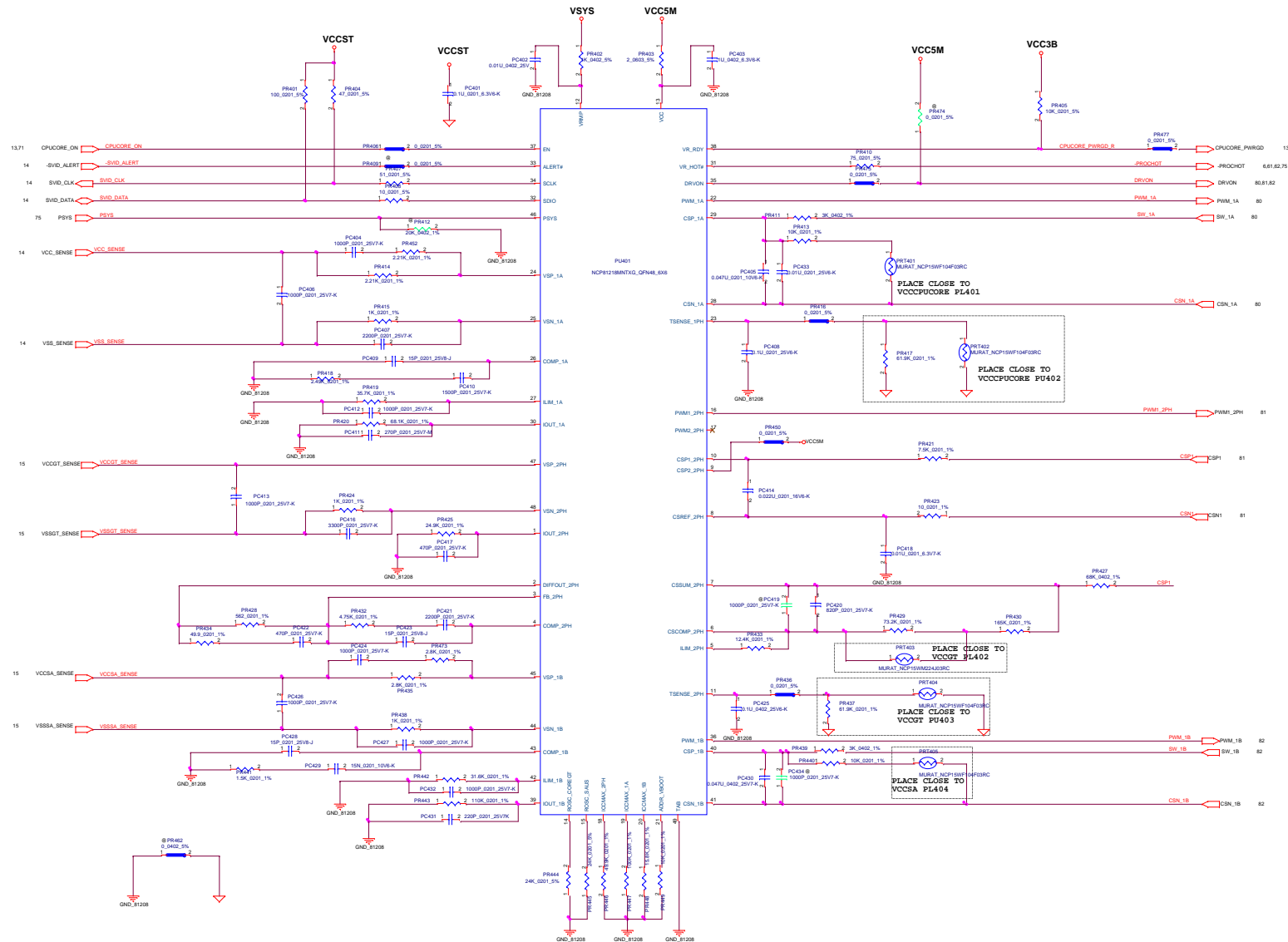
All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

VCC5M
TDC= 8A
OCP =12A

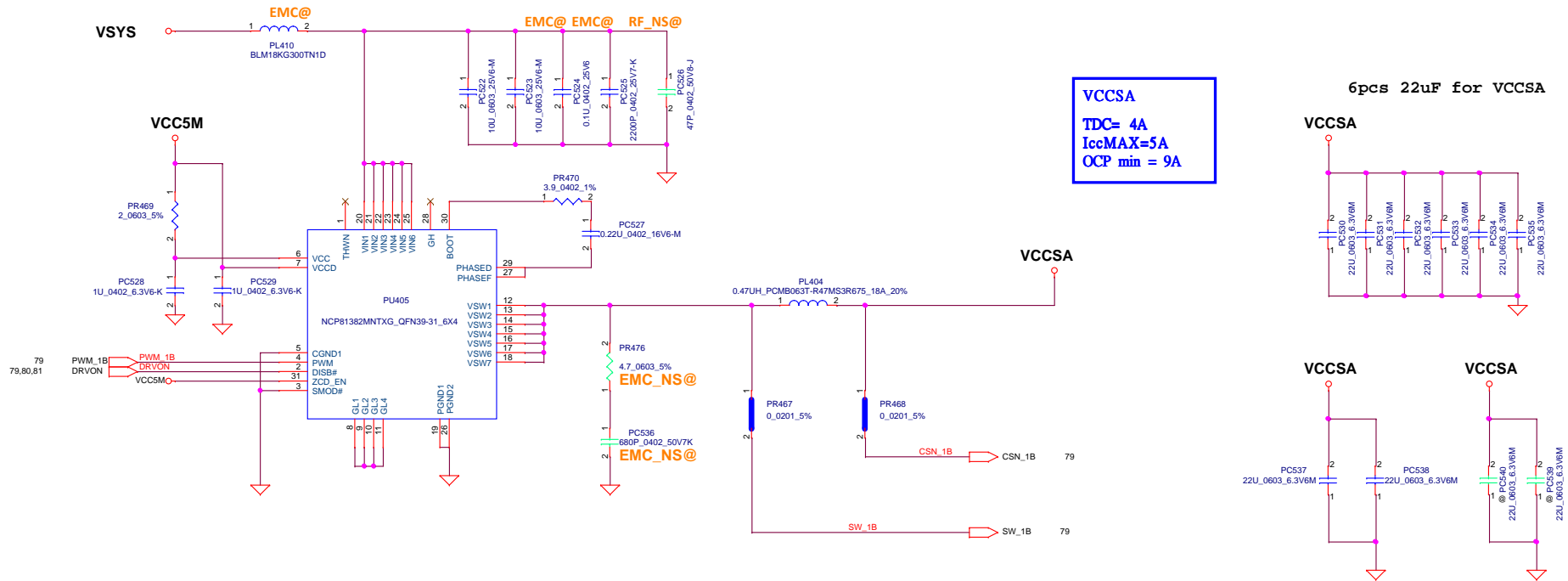
VCC3M
TDC= 8A
OCP =12A



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Size	Document Number	WV4 Intel		Rev 0.1	
Date	Tuesday, December 20, 2016	Sheet	78	of 100	

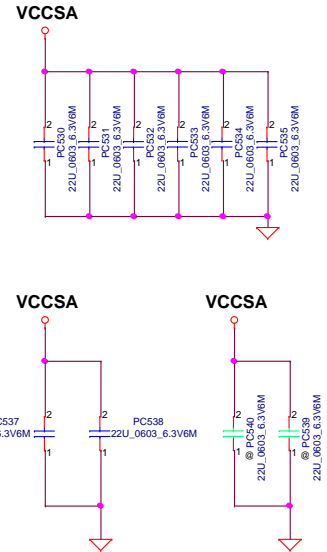



All the input MLCCs must be placed symmetrically on Top and Bottom.





VCCSA
TDC= 4A
IccMAX=5A
OCP min = 9A

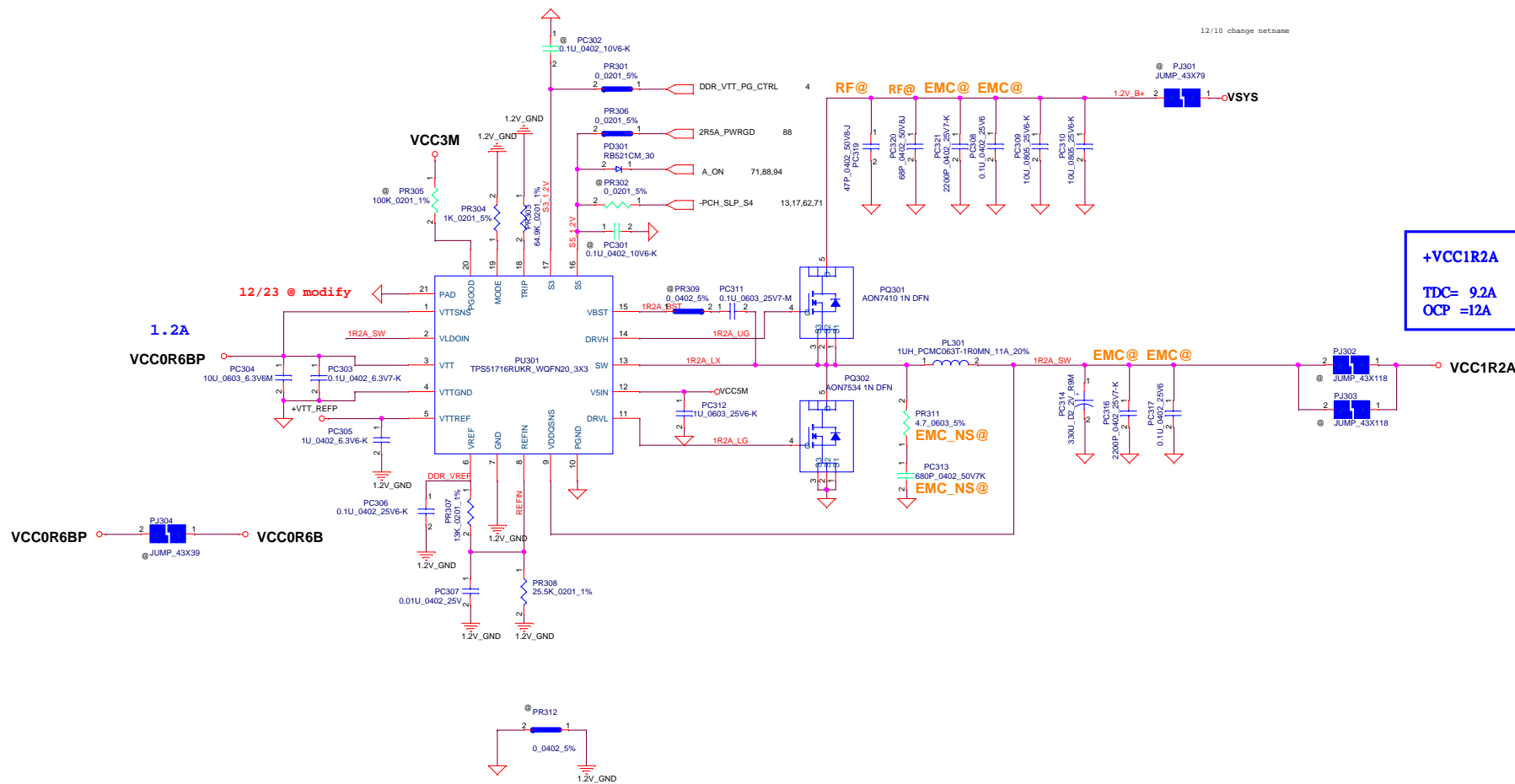
6pcs 22uF for VCCSA



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				Rev	
				0.1	
Date:				Tuesday, December 20, 2016	
Sheet				82 of 100	

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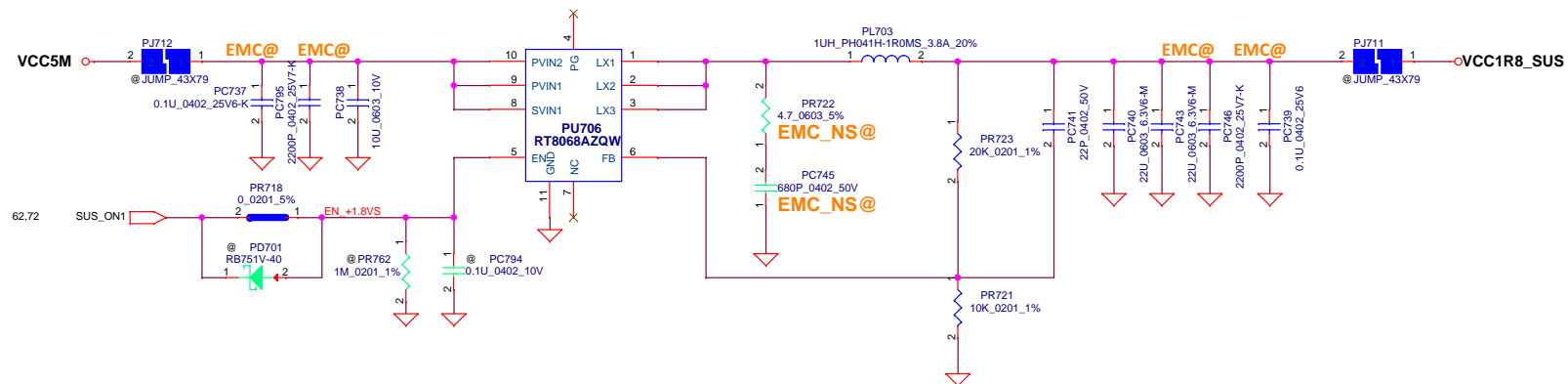
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				Custom		0.1	
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Issued Date		Deciphered Date		DC/DC VCC1R2A(TPS51716)	
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				WV4 Intel	
				Date:	Tuesday, December 20, 2016
				Sheet	85 of 100




Rev 0.1

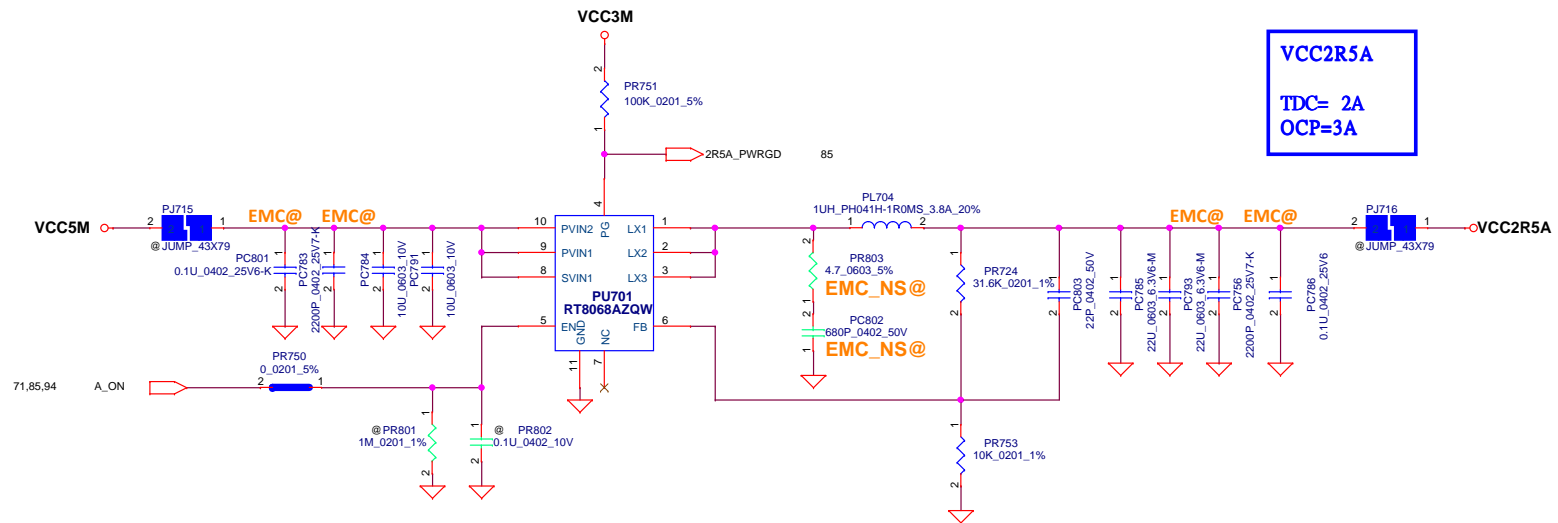


VCC1R8_SUS
TDC= 1A

Security Classification	LC Future Center Secret Data			Title	DC/DC VCC1R8_SUS(RT8068A)		
Issued Date		Deciphered Date		Size	Document Number	Rev	
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				Date:	Tuesday, December 20, 2016	Sheet 86 of 100	

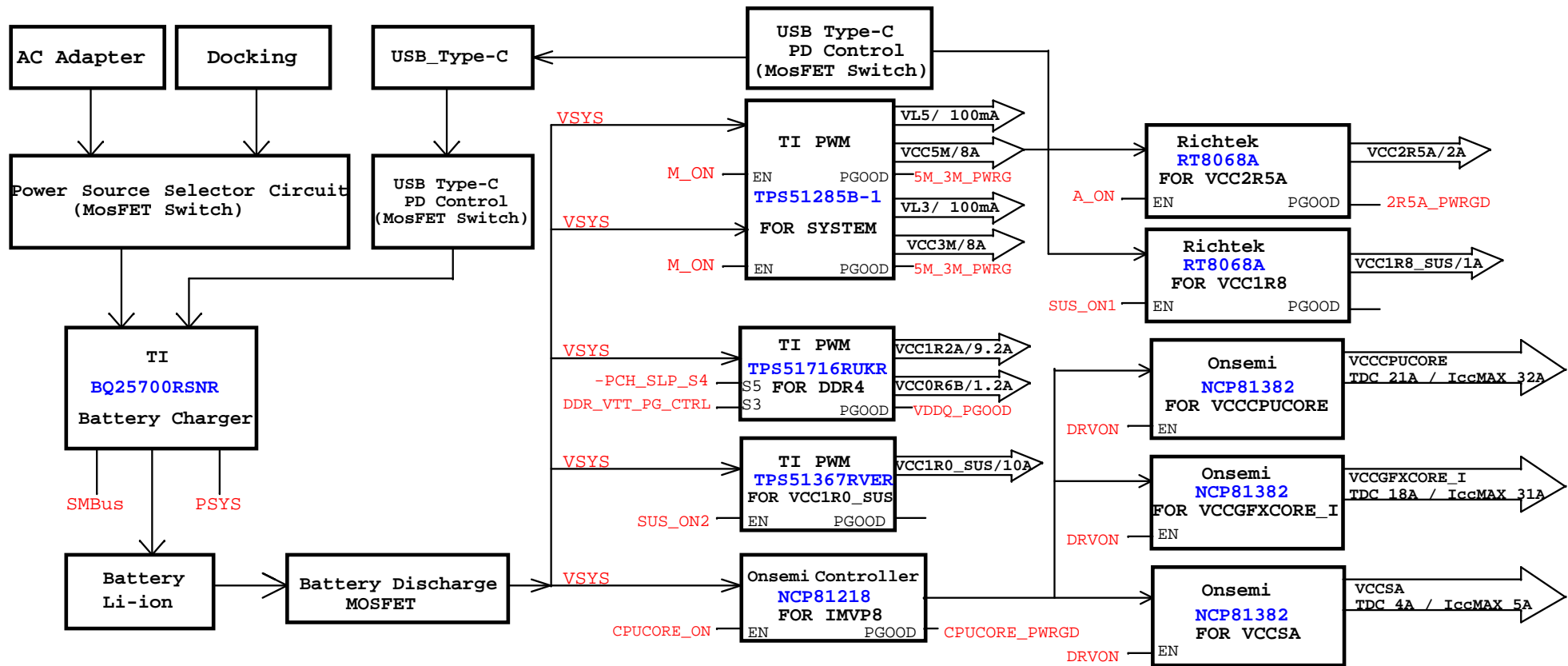
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				Custom		0.1	
Date:				Tuesday, December 20, 2016			
Sheet				57 of 100			





Security Classification	LC Future Center Secret Data			Title	DC/DC VCC2R5A(RT8068A)	
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				Date:	Tuesday, December 20, 2016	Sheet 88 of 100




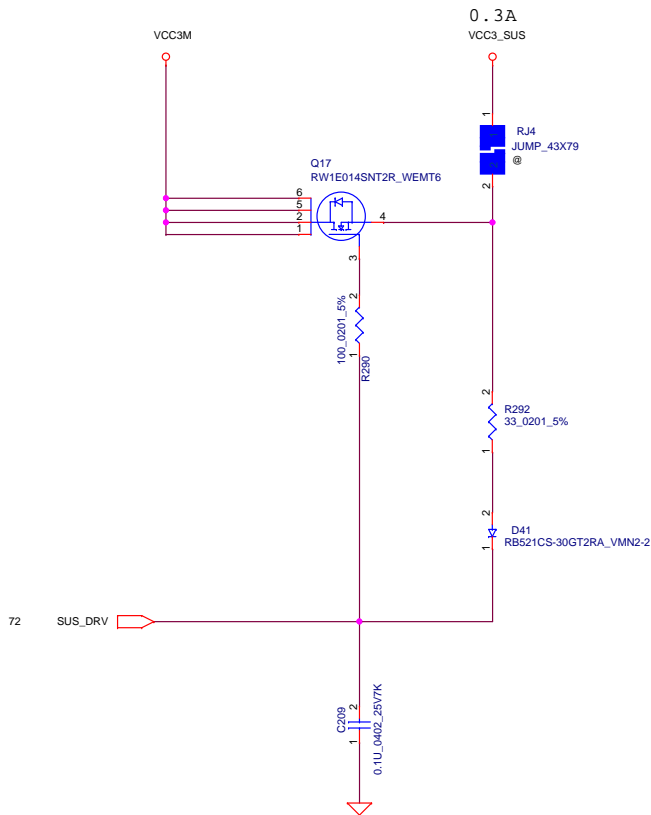


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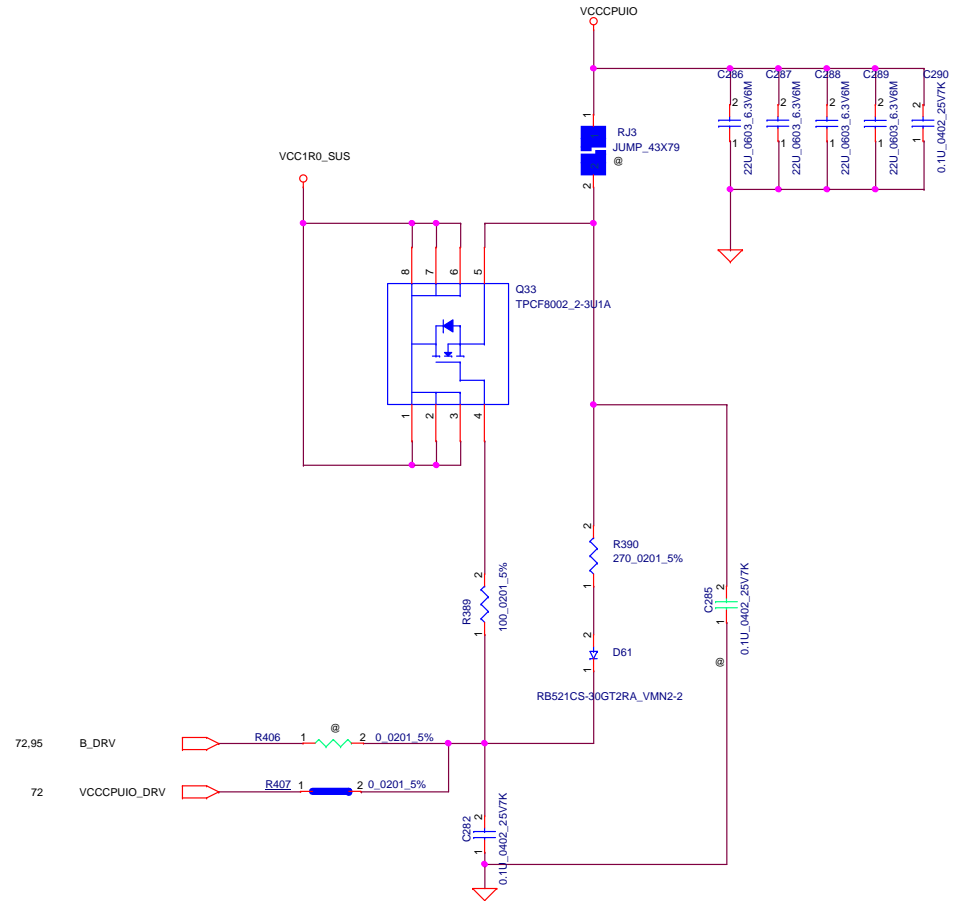
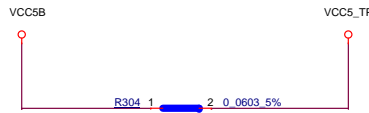
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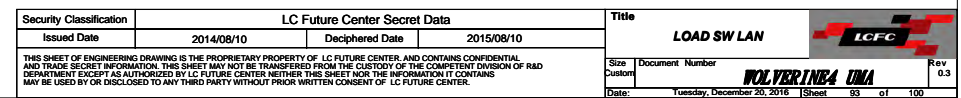
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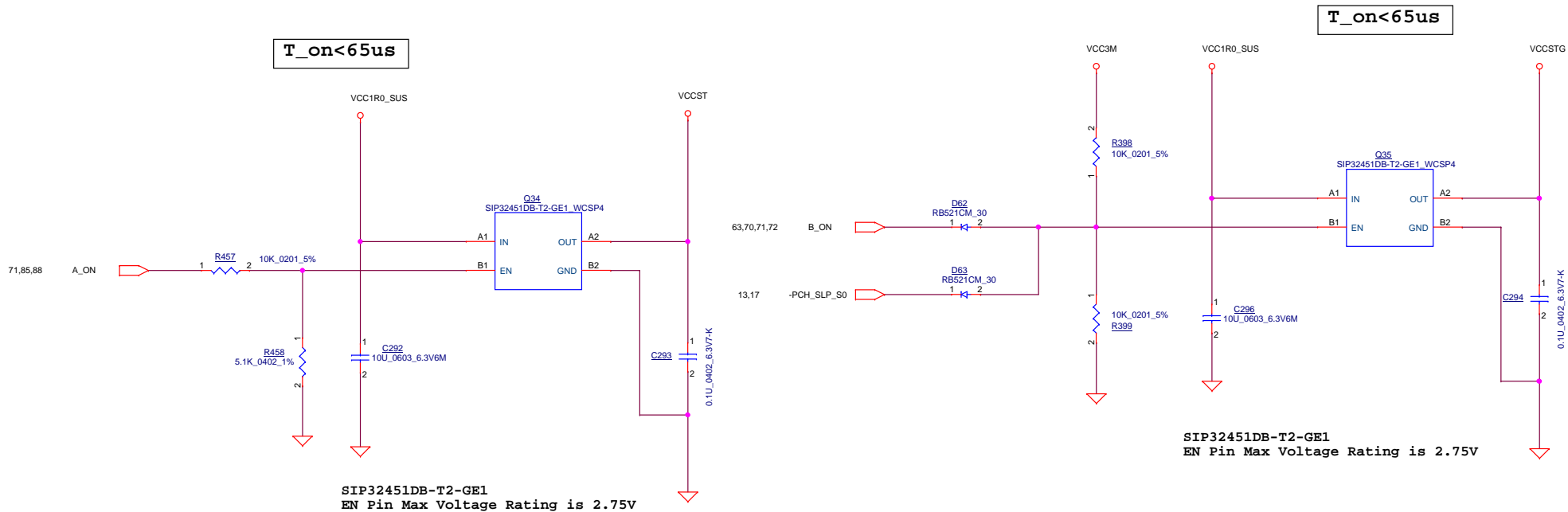



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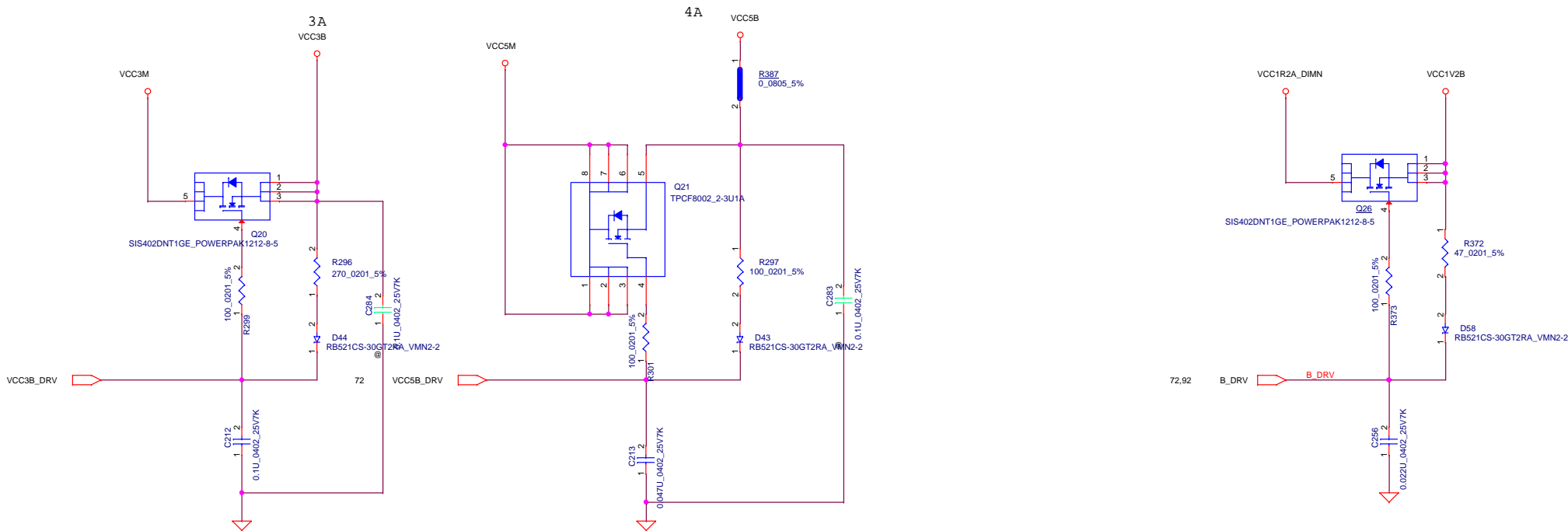
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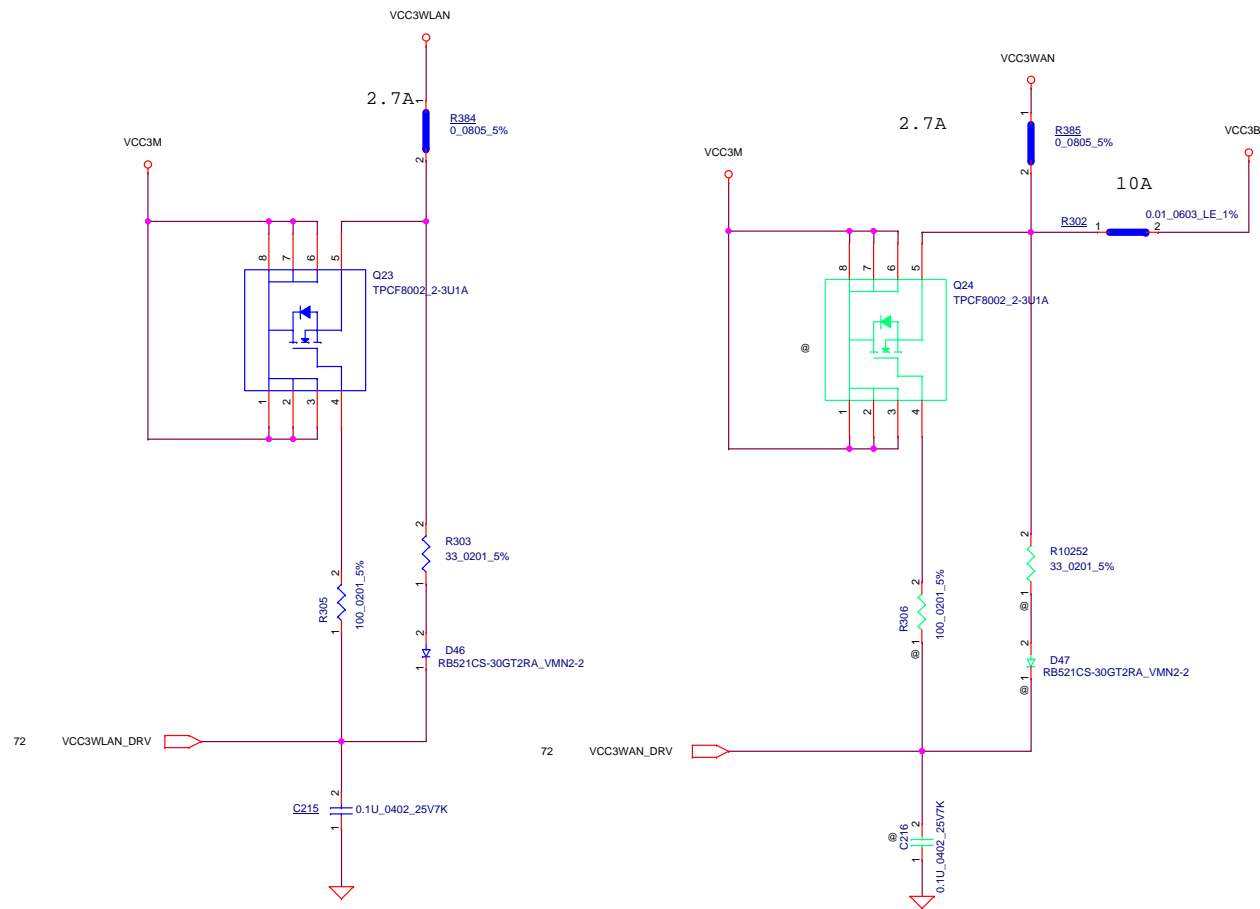




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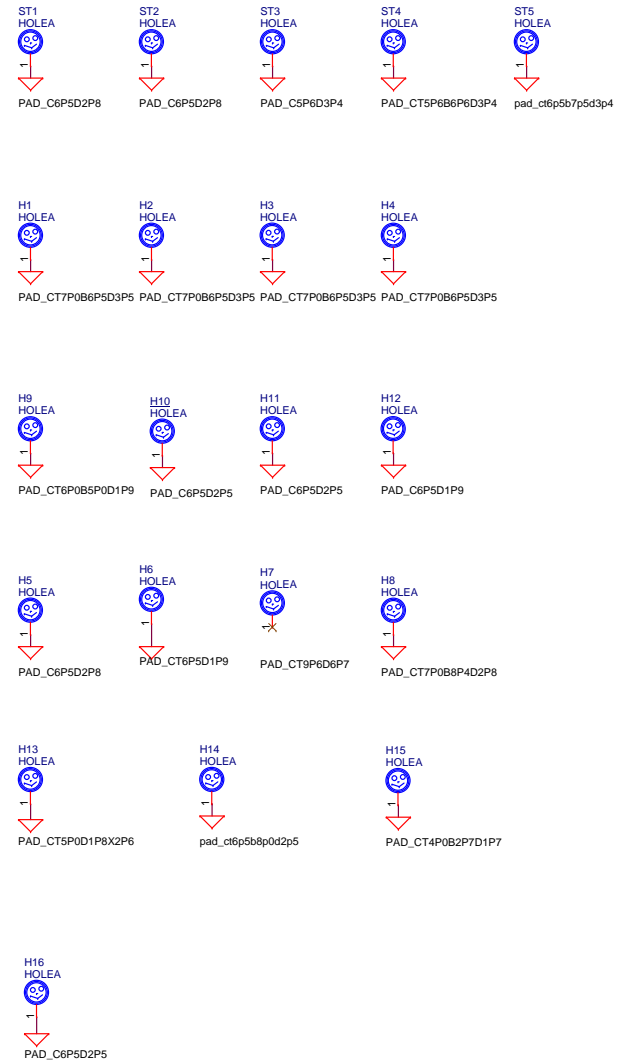
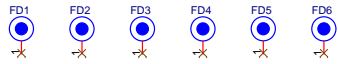
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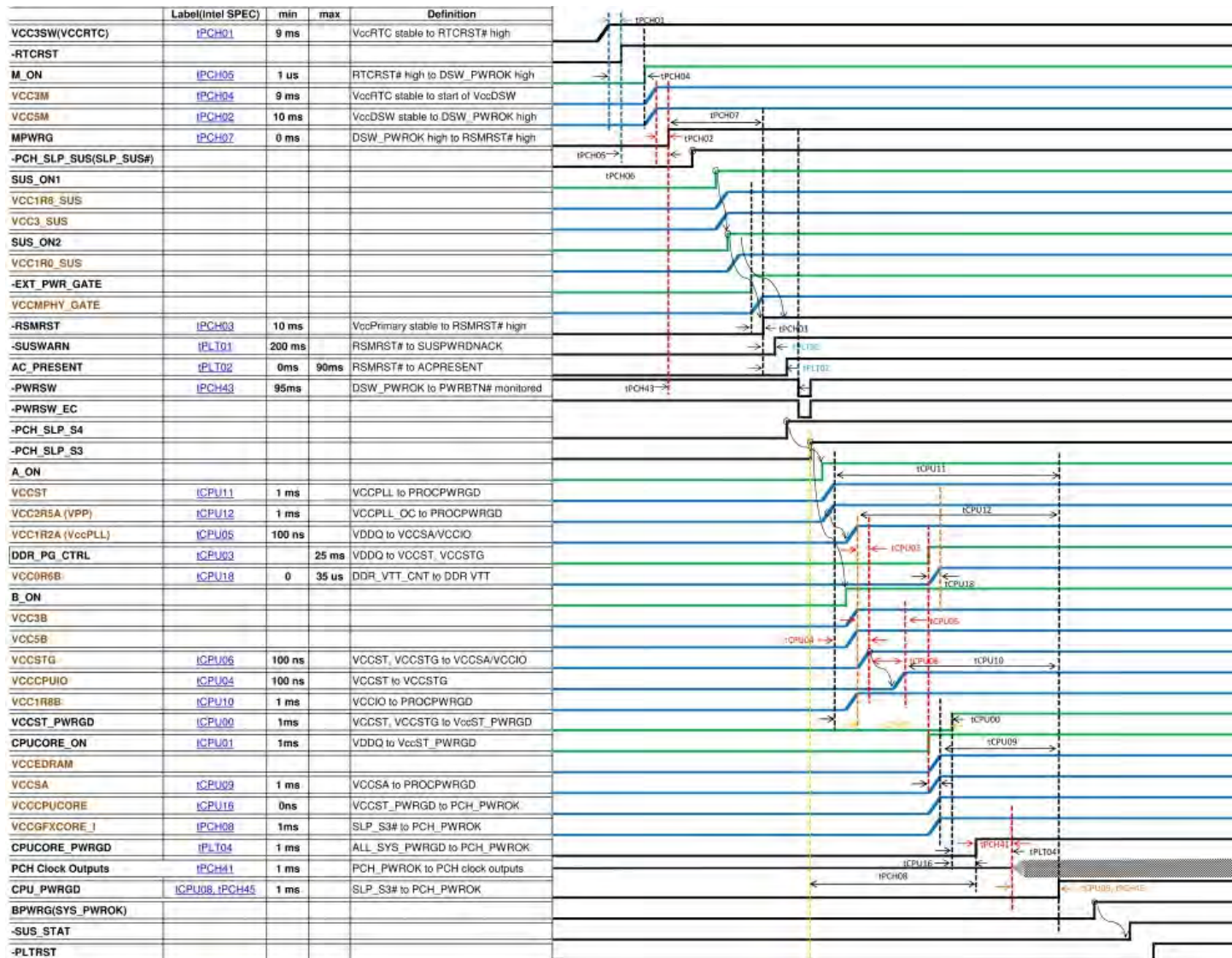
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