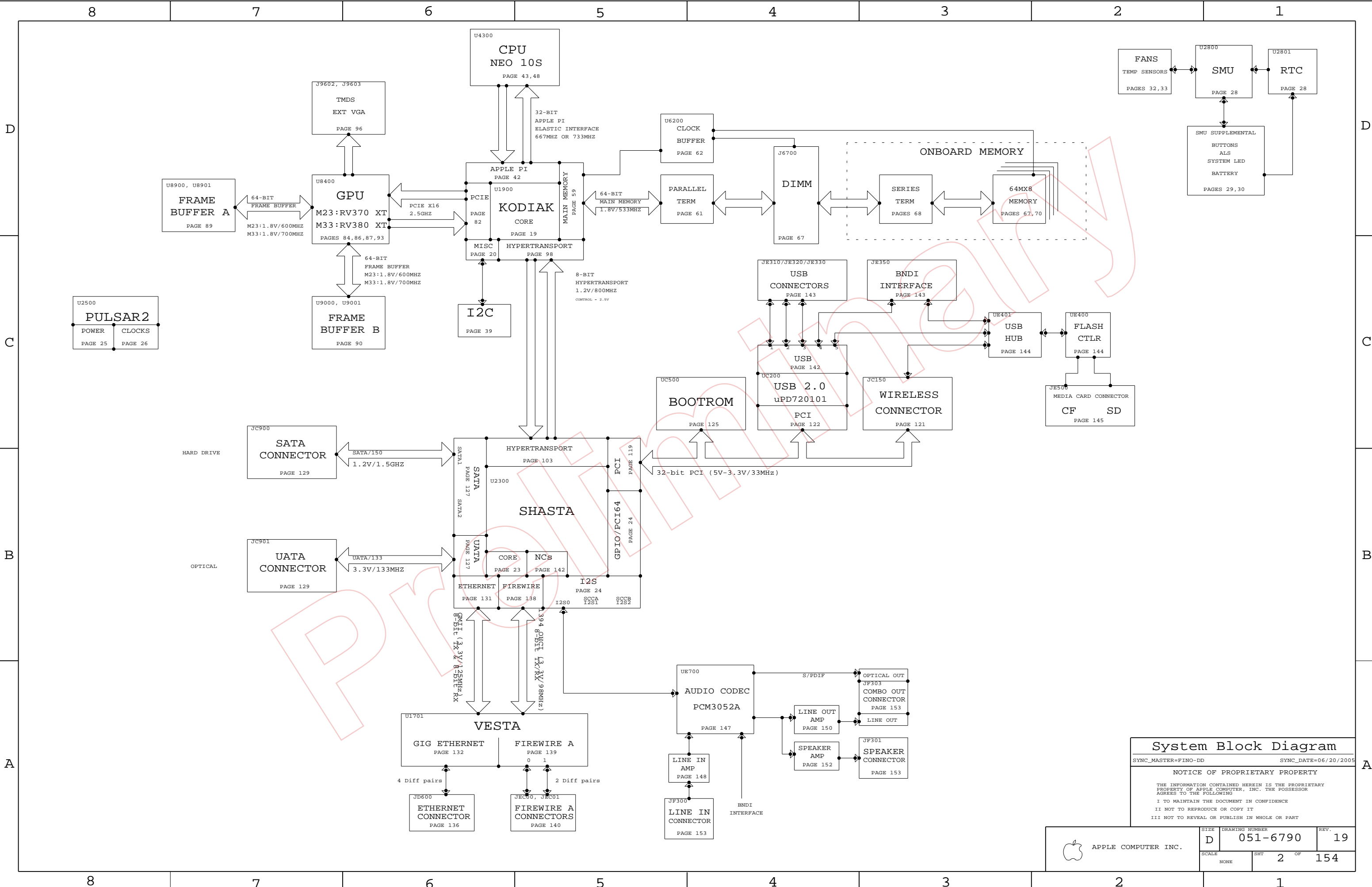


8		7		6		5		4		3		2		1				
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.												REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD	
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.																DATE	DATE	
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.												19		397409	ENGINEERING RELEASED	08/30/05	?	
FINO M23																		
DVT2 - 8/30/05																		
D	PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE
	2	2	System Block Diagram	FINO-DD		06/20/2005	38	54	CPU AVDD VREG	FINO-HS		06/20/2005	74	132	Vesta Ethernet PHY	Q63		08/01/2005
	3	4	Power Block Diagram	FINO-PC		06/20/2005	39	55	T,V,I SENSORS	FINO-HS		06/20/2005	75	136	ETHERNET CONNECTOR	FINO-DC		06/20/2005
	4	5	Table Items	FINO-DD		06/20/2005	40	56	CPU ALIASES & MISC	FINO-HS		06/20/2005	76	138	Shasta FireWire	Q63		08/01/2005
	5	6	FUNC TEST 1 OF 2	FINO-ME		06/20/2005	41	58	KODIAC NBMEM PWR & CAPS	Q63		08/01/2005	77	139	Vesta FireWire PHY	Q63		08/01/2005
	6	7	Power Conn / Alias	M23-PC		06/20/2005	42	59	Kodiak Memory Dq/Ctl	FINO-DS		06/20/2005	78	140	FIREWIRE CONNECTORS	FINO-DC		06/20/2005
	7	8	Signal Alias	FINO-DD		06/20/2005	43	61	Parallel Term	FINO-DS		06/20/2005	79	142	USB Host Interfaces	Q63		07/05/2005
	8	9	FUNC TEST 2 OF 2	FINO-ME		06/20/2005	44	62	Main Memory Clock Buffer	FINO-DS		06/20/2005	80	143	USB Device Interfaces	FINO-PC		06/20/2005
	9	11	1.8V Vreg	M23-PC		06/20/2005	45	63	MEMORY ADDR BRANCHING	FINO-DS		06/20/2005	81	144	Flash Media Ctrl	FINO-PC		06/20/2005
	10	12	1.5V Vreg	FINO-PC		06/20/2005	46	67	Memory Dimm A	FINO-DS		06/20/2005	82	145	Flash Connector	FINO-PC		06/20/2005
C	11	13	1.2V Vreg	FINO-PC		06/20/2005	47	68	MLB Mem Series Term	FINO-DS		06/20/2005	83	147	AUDIO: CODEC	FINO-SO		08/01/2005
	12	15	2.5V Vreg	FINO-PC		06/20/2005	48	69	On-Board DDR SDRAM	FINO-DS		06/20/2005	84	148	AUDIO: LINE INPUT AMP	FINO-SO		08/01/2005
	13	16	5V & 3.3V Fets	FINO-PC		06/20/2005	49	70	On-Board DDR SDRAM	FINO-DS		06/20/2005	85	150	AUDIO: LINE OUT AMP	FINO-SO		08/01/2005
	14	17	Vesta Core / Misc	FINO-DC		06/20/2005	50	82	KODIAK PCI-E X16	Q63		08/01/2005	86	152	AUDIO: SPEAKER AMP	FINO-SO		08/01/2005
	15	19	KODIAK CORE & BYPASS	Q63		08/01/2005	51	84	GPU PCIe	FINO-DD		06/20/2005	87	153	AUDIO: CONNECTORS	FINO-SO		08/01/2005
	16	20	KODIAK & SHASTA MISC	FINO-ME		06/20/2005	52	85	Graphics Vregs	M23-DD		06/20/2005	88	154	AUDIO: POWER SUPPLIES	FINO-SO		08/01/2005
	17	23	Shasta Core Power	Q63		08/01/2005	53	86	GPU Core Power	FINO-DD		06/20/2005						
	18	24	Shasta Serial / Misc	FINO-ME		06/20/2005	54	87	GPU Frame Buffer	FINO-DD		06/20/2005						
	19	25	PULSAR2 POWER	Q63		08/01/2005	55	88	FB Series Termination	FINO-DD		06/20/2005						
	20	26	PULSAR2 CLOCKS	FINO-ME		06/20/2005	56	89	GPU GDDR SDRAM A	FINO-DD		06/20/2005						
B	21	27	Pulsar Aliases	FINO-ME		06/20/2005	57	90	GPU GDDR SDRAM B	FINO-DD		06/20/2005						
	22	28	System Management Unit	Q63		08/01/2005	58	92	GPU Straps	FINO-DD		06/20/2005						
	23	29	SMU SUPPLEMENTAL (2)	FINO-HS		06/20/2005	59	93	GPU DVI & DACs	FINO-DD		06/20/2005						
	24	30	SMU SUPPLEMENTAL (3)	FINO-HS		06/20/2005	60	96	TMDS/Inverter/ExtVGA	M23-DD		06/20/2005						
	25	31	SMU SUPPLEMENTAL (4)	FINO-HS		06/20/2005	61	97	KODIAK PCI-E CONST	FINO-DD		06/20/2005						
	26	32	Fan 0, 1 & System Temp	FINO-HS		06/20/2005	62	98	KODIAK HT16	Q63		08/01/2005						
	27	33	Fan 2 & HD Temp	FINO-HS		06/20/2005	63	101	HT ALIASES	FINO-ME		06/20/2005						
	28	39	I2C Connections	FINO-ME		06/20/2005	64	103	Shasta HyperTransport	Q63		08/01/2005						
	29	41	KODIAK EI PWR & CAPS	Q63		08/01/2005	65	119	Shasta PCI Interface	Q63		08/01/2005						
	30	42	KODIAK EI A	Q63		08/01/2005	66	120	PCI SERIES TERMINATION	FINO-MW		06/20/2005						
A	31	43	CPU EI AND IO	FINO-HS		06/20/2005	67	121	AIRPORT & BLUETOOTH	FINO-MW		06/20/2005						
	32	44	KODIAK EI B	Q63		08/01/2005	68	122	USB 2.0 PCI Interface	Q63		08/01/2005						
	33	47	CPU STRAPS	FINO-HS		06/20/2005	69	125	BootROM	Q63		08/01/2005						
	34	48	CPU POWER AND BYPASS	FINO-HS		06/20/2005	70	127	Shasta Disk	M23-DC		06/20/2005						
	35	49	PROC DECOUPLING	FINO-HS		06/20/2005	71	129	Disk Connectors	M23-DC		06/20/2005						
	36	50	CPU VCORE VREG	M23-HS		06/20/2005	72	130	ENET SERIES TERM	FINO-DC		06/20/2005						
	37	52	CPU VCORE MORE BYPASS	FINO-HS		06/20/2005	73	131	Shasta Ethernet	Q63		08/01/2005						
8		7		6		5		4		3		2		1				
												DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.		
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														SCALE		SCH,MLB,FINO,M23		
														NONE		DRAWING NUMBER		
														MATERIAL/FINISH NOTED AS APPLICABLE		051-6790		
														SIZE D		REV. 19		
																SHT 1 OF 154		



System Block Diagram

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

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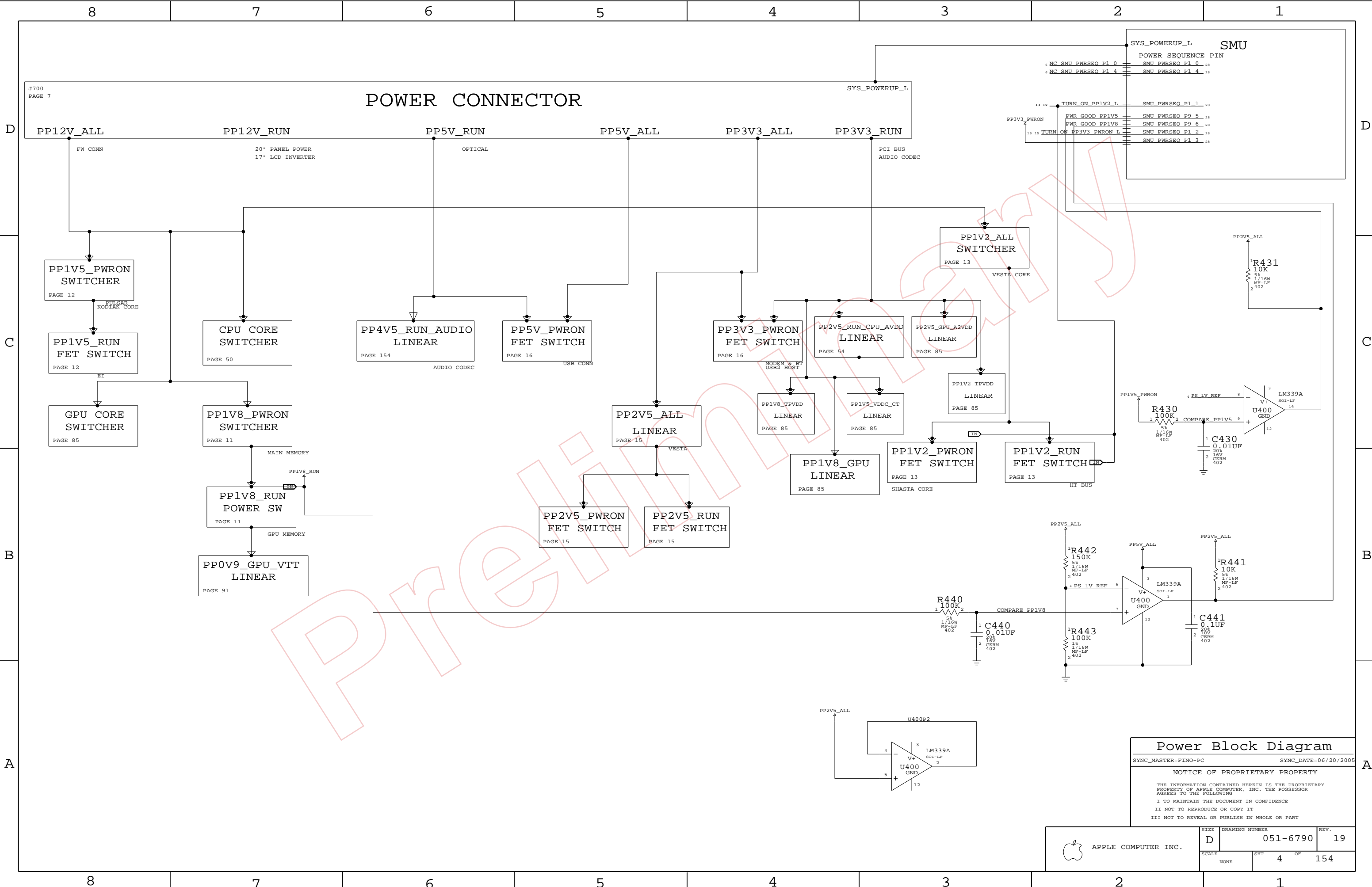
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	D	051-6790	19
SCALE		SHT	2 OF 154
NONE			



Power Block Diagram

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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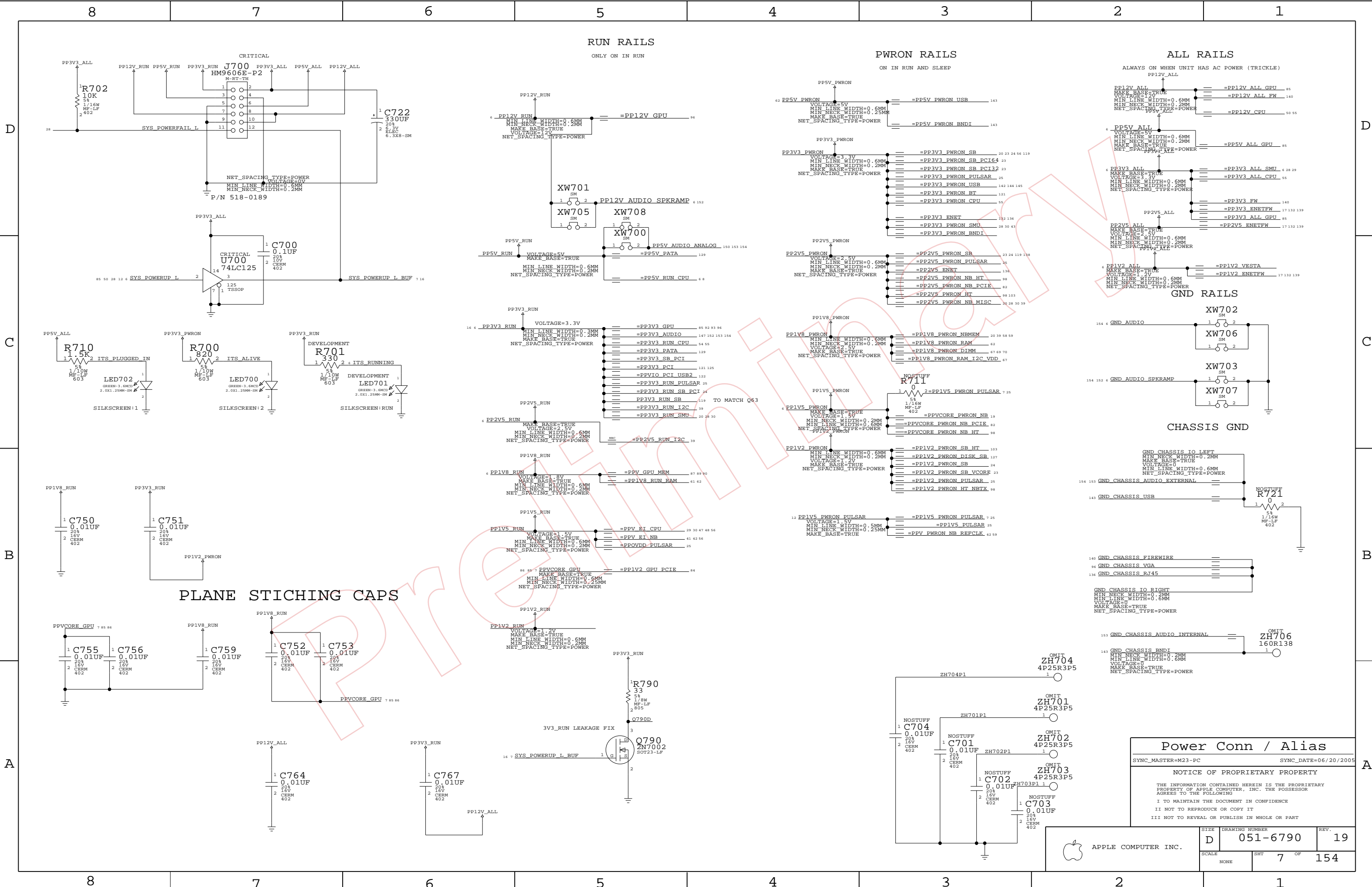
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	OF
NONE		4	154

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<table><tr><th>PART #</th><th>QTY</th><th>DEVICE</th><th>PACKAGE</th><th>DESCRIPTION</th><th>VALUE</th><th>VOLT.</th><th>WATT.</th><th>TOL.</th><th>REFERENCE DESIGNATOR(S)</th><th>BOM OPTION</th></tr><tr><td>337S3224</td><td>1</td><td>PROCESSOR</td><td>CBGA-576-1MM</td><td>IC,GPUL,DD3.1,1.9G,85C</td><td>1.9GHZ</td><td>1.10V</td><td>45W</td><td>50MV</td><td>U4300</td><td>17_INCH_LCD</td></tr><tr><td>337S3220</td><td>1</td><td>PROCESSOR</td><td>CBGA-576-1MM</td><td>IC,GPUL,DD3.1,2.1G,85C</td><td>2.1GHZ</td><td>1.10V</td><td>45W</td><td>50MV</td><td>U4300</td><td>20_INCH_LCD</td></tr></table>												PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION	337S3224	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,1.9G,85C	1.9GHZ	1.10V	45W	50MV	U4300	17_INCH_LCD	337S3220	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.1G,85C	2.1GHZ	1.10V	45W	50MV	U4300	20_INCH_LCD	CRITICAL		CRITICAL																																																											
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337S3231	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.30V																																																																																																						
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603-7321	1	M33 CPU HEATSINK	MECH1	20_INCH_LCD																																																																																																						
603-7319	1	M23 GPU HEATSINK	MECH2	17_INCH_LCD																																																																																																						
603-7322	1	M33 GPU HEATSINK	MECH2	20_INCH_LCD																																																																																																						
603-7320	1	M23 NB HEATSINK	MECH3	17_INCH_LCD																																																																																																						
603-7323	1	M33 NB HEATSINK	MECH3	20_INCH_LCD																																																																																																						
875-1905	1	CPU GAP FILLER	GAP1																																																																																																							
860-0708	2	M33 ODD NUTS	SDFC900,SDFC901	20_INCH_LCD																																																																																																						
ALTERNATES																																																																																																										
<table><tr><th>PART NUMBER</th><th>ALTERNATE FOR PART NUMBER</th><th>BOM OPTION</th><th>REF DES</th><th>COMMENTS:</th></tr><tr><td>378S0140</td><td>378S0141</td><td></td><td>LED700,LED702</td><td>KINGBRIGHT LED</td></tr><tr><td>343S0388</td><td>343S0356</td><td></td><td>U1701</td><td>VESTA A4</td></tr><tr><td>126S0078</td><td>126S0086</td><td></td><td>C722</td><td>EL CAP</td></tr><tr><td>126S0068</td><td>126S0088</td><td></td><td>CF000</td><td>EL CAP</td></tr></table>												PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	378S0140	378S0141		LED700,LED702	KINGBRIGHT LED	343S0388	343S0356		U1701	VESTA A4	126S0078	126S0086		C722	EL CAP	126S0068	126S0088		CF000	EL CAP																																																																						
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Table Items												SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005																																																																																														
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8		7		6		5		4		3		2		1																																																																																												

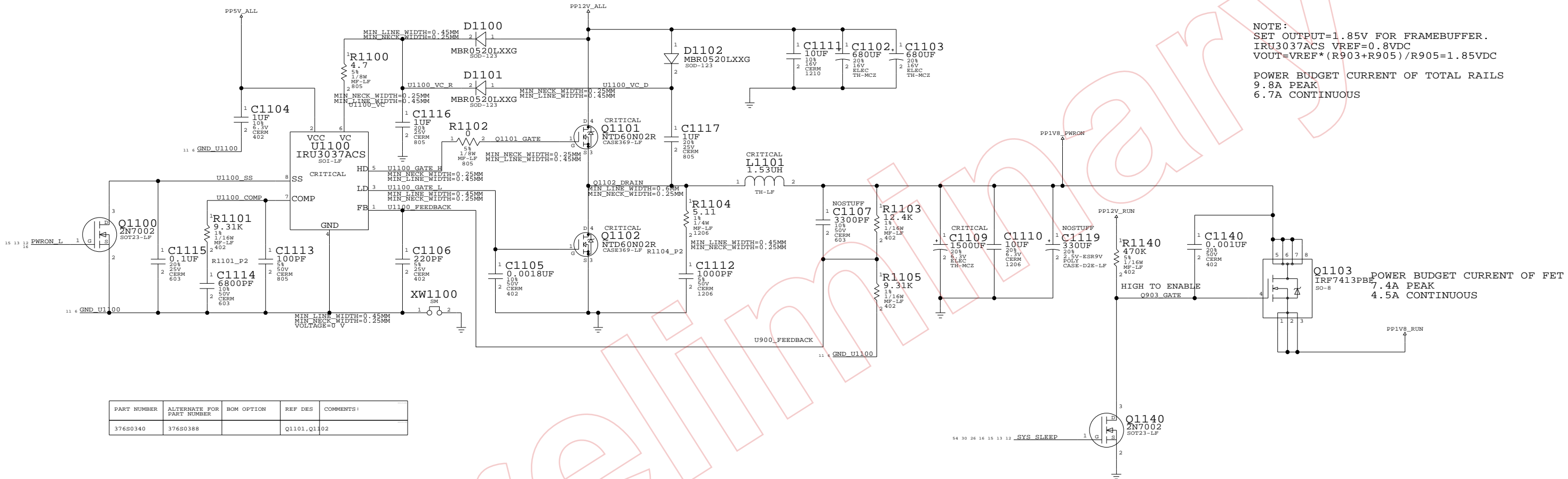
8	7	6	5	4	3	2	1
NO TEST XW NETS							
<div><div>NO TEST=YESGND U110011</div><div>NO TEST=YESGND U120012</div><div>NO TEST=YESGND U130013</div><div>NO TEST=YESPP 2V5PWRONNBMIC20</div><div>NO TEST=YESPP 1V2PWRONSBVCORE23</div><div>NO TEST=YESPP 3V3PWRONSBPC16423</div><div>NO TEST=YESPP 2V5PWRONSB23</div><div>NO TEST=YESPP 1V2PWRONSBELL45VDD24</div><div>NO TEST=YESPP OVDD PULSAR125</div><div>NO TEST=YESPP 1V2PWRONPULSAR125</div><div>NO TEST=YESPP 1V5PULSAR225</div><div>NO TEST=YESPP 1V5PWRONPULSAR225</div><div>NO TEST=YESGND SMU AVSS28 55</div><div>NO TEST=YESPP 3V3ALLSMUAVCC28</div><div>NO TEST=YESPP 3V3ALLSMU28</div><div>NO TEST=YESPP VEINB41</div><div>NO TEST=YESGND CPU AVDD48</div><div>NO TEST=YESVC AGND50</div><div>NO TEST=YESVC OUTSEN R50</div><div>NO TEST=YESKPDVD2 FMAX55</div><div>NO TEST=YESGND GPU PVSS86</div><div>NO TEST=YESGND GPU MPVSS87</div><div>NO TEST=YESGND AUDIO MIC153 154</div></div>	<div><div>NO TEST=YESGND GPU TPVSS93</div><div>NO TEST=YESGND GPU TVVSSR93</div><div>NO TEST=YESGND GPU VSSD193</div><div>NO TEST=YESGND GPU AVSSN93</div><div>NO TEST=YESGND GPU AVSSQ93</div><div>NO TEST=YESGND GPU A2VSSN93</div><div>NO TEST=YESGND GPU A2VSSQ93</div><div>NO TEST=YESKOD L15 GND98 101</div><div>NO TEST=YESPP 3V3SBPCI B998</div><div>NO TEST=YESPP 2V5PWRONSB B9119</div><div>NO TEST=YESPP VIOPCIUSB2 C2122</div><div>NO TEST=YESPP 1V2PWRONDISKSB CC127</div><div>NO TEST=YESPP2V5 VESTA BIASVDD1132</div><div>NO TEST=YESPP2V5 VESTA XTALVDD1132</div><div>NO TEST=YESPP1V2 VESTA PLLVDD1132</div><div>NO TEST=YESPP1V2 VESTA PLLVDD2139</div><div>NO TEST=YESPP2V5 VESTA BIASVDD2139</div><div>NO TEST=YESPP2V5 VESTA XTALVDD2139</div><div>NO TEST=YESPP1V2 VESTA FAVDDL139</div><div>NO TEST=YESPP2V5 VESTA FAVDDM139</div><div>NO TEST=YESPP3V3 VESTA FAVDDH139</div><div>NO TEST=YESPP3V3 PWRON NEC AVDD142</div><div>NO TEST=YESGND AUD LOAMP150 154</div></div>	<div><div>NO TEST=YESGND NEC AVSS R142</div><div>NO TEST=YESGND AUDIO SPKRAMP PLANE152 154</div><div>NO TEST=YESGND AUDIO CODEC147 148 150 154</div><div>NO TEST=YESKPGND2 FMAX95</div><div>NO TEST=YESTDIODE POS FMAX95</div><div>NO TEST=YESTDIODE NEG FMAX95</div><div>NO TEST=YESDAGND95</div><div>NO TEST=YESINA138 OUT95</div><div>NO TEST=YESRAMCLK AVSS62</div><div>NO TEST=YESPP12V AUDIO SPKRAMP7152</div><div>NO TEST=YESGND AUDIO7154</div><div>NO TEST=YESGND AUDIO SPKRAMP7152 154</div><div>NO TEST=YESKOD H05 GND82 97</div><div>NO TEST=YESKOD K07 GND82 97</div><div>NO TEST=YESKOD G10 GND82 97</div><div>NO TEST=YESPP2V5 VESTA BIASVDD282 97</div><div>NO TEST=YESKOD J13 GND82 97</div><div>NO TEST=YESKOD L13 GND82 97</div><div>NO TEST=YESKOD H08 GND82 97</div><div>NO TEST=YESPCIE SLOTA PRSNT L82 84</div><div>NO TEST=YESU8500 GND85</div><div>NO TEST=YESGND AUD LOAMP CHGPMPL50 154</div></div>	<div><div>NO TEST=YESTP FBBCS1 L87</div><div>NO TEST=YESAUD 4V5 FB154</div><div>NO TEST=YESITS RUNNING7</div><div>NO TEST=YESLED801 I8</div><div>NO TEST=YESLED802 I8</div><div>NO TEST=YESPCI CLK66M SB INT R26</div><div>NO TEST=YESQ800 D8</div><div>NO TEST=YESQ800 G8</div><div>NO TEST=YESQ801 B8</div><div>NO TEST=YESQ802 B8</div><div>NO TEST=YESQ802 E8</div><div>NO TEST=YESQ803 B8</div><div>NO TEST=YESTP USB2 PWREN<0>143</div><div>NO TEST=YESTP USB2 PWREN<1>143</div><div>NO TEST=YESTP SB FSTEST24</div><div>NO TEST=YESTP SB PLLTEST24</div><div>NO TEST=YESTP USB2 PWREN<2>143</div><div>NO TEST=YESTP USB2 PWREN<3>143</div><div>NO TEST=YESTP USB2 PWREN<4>143</div><div>NO TEST=YESTP NEC NTEST1122</div><div>NO TEST=YESTP NEC SMC122</div><div>NO TEST=YESTP NEC SMI L102</div><div>NO TEST=YESTP NEC SRCLK102</div><div>NO TEST=YESTP NEC SRMOD122</div><div>NO TEST=YESTP NEC TEST122</div><div>NO TEST=YESUATA DASP L DS129</div><div>NO TEST=YESRFBDC19>88 89</div><div>NO TEST=YESRFBDC18>88 89</div><div>NO TEST=YESRFBDC16>88 89</div><div>NO TEST=YESRFBDC15>88 89</div><div>NO TEST=YESRFBDC14>88 89</div><div>NO TEST=YESRFBDC13>88 89</div><div>NO TEST=YESRFBDC11>88 89</div><div>NO TEST=YESRFBDC10>88 89</div><div>NO TEST=YESRFBDC8>88 89</div><div>NO TEST=YESRFBDC7>88 89</div><div>NO TEST=YESRFBDC6>88 89</div><div>NO TEST=YESRFBDC5>88 89</div><div>NO TEST=YESRFBDC3>88 89</div><div>NO TEST=YESRFBDC2>88 89</div><div>NO TEST=YESRFBDC1>88 89</div><div>NO TEST=YESRAM DQ R<63>61 68 70</div><div>NO TEST=YESRAM DQ R<60>61 68 70</div><div>NO TEST=YESRAM DQ R<59>61 68 70</div><div>NO TEST=YESRAM DQ R<58>61 68 70</div><div>NO TEST=YESRAM DQ R<57>61 68 70</div><div>NO TEST=YESRAM DQ R<56>61 68 70</div><div>NO TEST=YESRAM DQ R<54>61 68 70</div><div>NO TEST=YESRAM DQ R<53>61 68 70</div><div>NO TEST=YESRAM DQ R<52>61 68 70</div><div>NO TEST=YESRAM DQ R<50>61 68 70</div><div>NO TEST=YESRAM DQ R<49>61 68 70</div><div>NO TEST=YESRAM DQ R<48>61 68 70</div><div>NO TEST=YESRAM DQ R<46>61 68 70</div><div>NO TEST=YESRAM DQ R<45>61 68 70</div><div>NO TEST=YESRAM DQ R<44>61 68 70</div><div>NO TEST=YESRAM DQ R<43>61 68 70</div><div>NO TEST=YESRAM DQ R<41>61 68 70</div><div>NO TEST=YESRAM DQ R<40>61 68 70</div><div>NO TEST=YESRAM DQ R<37>61 68 70</div><div>NO TEST=YESRAM DQ R<36>61 68 70</div><div>NO TEST=YESRAM DQ R<34>61 68 70</div><div>NO TEST=YESRAM DQ R<33>61 68 70</div><div>NO TEST=YESRAM DQ R<32>61 68 70</div><div>NO TEST=YESRAM DQ R<30>61 68 69</div><div>NO TEST=YESRAM DQ R<29>61 68 69</div><div>NO TEST=YESRAM DQ R<28>61 68 69</div><div>NO TEST=YESRAM DQ R<22>61 68 69</div><div>NO TEST=YESRAM DQ R<21>61 68 69</div><div>NO TEST=YESRAM DQ R<20>61 68 69</div><div>NO TEST=YESRAM DQ R<19>61 68 69</div><div>NO TEST=YESRAM DQ R<17>61 68 69</div><div>NO TEST=YESRAM DQ R<16>61 68 69</div><div>NO TEST=YESRAM DQ R<14>61 68 69</div><div>NO TEST=YESRAM DQ R<13>61 68 69</div><div>NO TEST=YESRAM DQ R<12>61 68 69</div><div>NO TEST=YESRAM DQ R<11>61 68 69</div></div>	<div><div>FUNC TEST=TRUESMU BOOT SCLK28 29</div><div>FUNC TEST=TRUESMU BOOT RXD28 29</div><div>FUNC TEST=TRUESMU BOOT CE28 29</div><div>FUNC TEST=TRUESMU BOOT CNVSS28 29</div><div>FUNC TEST=TRUESMU BOOT TXD28 29</div><div>FUNC TEST=TRUESMU BOOT BUSY28 29</div><div>FUNC TEST=TRUESMU MANUAL RESET L29</div><div>PP1V2_ALL FUNC TEST=TRUE</div><div>PP3V3_ALL FUNC TEST=TRUE</div><div>PP5V_ALL</div><div>PP1V8_RUN FUNC TEST=TRUE</div><div>PP2V5_RUN FUNC TEST=TRUE</div><div>PP3V3_RUN FUNC TEST=TRUE</div><div>PP12V_RUN</div><div>PP1V5_PWRON FUNC TEST=TRUE</div><div>GND FUNC TEST=TRUE</div></div>	<div><div>FUNC TEST=TRUESYS POWER BUTTON L28 29</div><div>FUNC TEST=TRUEPOWER_BUTTON_L29</div><div>FUNC TEST=TRUERESET_BUTTON_L29</div><div>FUNC TEST=TRUESMU RESET L28 29</div><div>FUNC TEST=TRUESYS POWERUP_L7 12 28 50 85</div><div>NO TEST=YESRAM DQ R<9>61 68 69</div><div>NO TEST=YESRAM DQ R<8>61 68 69</div><div>NO TEST=YESRAM DQ R<7>61 68 69</div><div>NO TEST=YESRAM DQ R<6>61 68 69</div><div>NO TEST=YESRAM DQ R<5>61 68 69</div><div>NO TEST=YESRAM DQ R<3>61 68 69</div><div>NO TEST=YESRAM DQ R<2>61 68 69</div><div>NO TEST=YESRAM DQ R<1>61 68 69</div><div>NO TEST=YESRAM DQ R<9>61 68 69</div><div>NO TEST=YESRAM DQ R<8>61 68 69</div><div>NO TEST=YESRAM DQ R<7>61 68 69</div><div>NO TEST=YESRAM DQ R<6>61 68 69</div><div>NO TEST=YESRAM DQ R<5>61 68 69</div><div>NO TEST=YESRAM DQ R<3>61 68 69</div><div>NO TEST=YESRAM DQ R<2>61 68 69</div><div>NO TEST=YESRAM DQ R<1>61 68 69</div><div>NO TEST=YESRAM DQ R<22>61 68 69</div><div>NO TEST=YESRAM DQ R<21>61 68 69</div><div>NO TEST=YESRAM DQ R<20>61 68 69</div><div>NO TEST=YESRAM DQ R<19>61 68 69</div><div>NO TEST=YESRAM DQ R<17>61 68 69</div><div>NO TEST=YESRAM DQ R<16>61 68 69</div><div>NO TEST=YESRAM DQ R<14>61 68 69</div><div>NO TEST=YESRAM DQ R<13>61 68 69</div><div>NO TEST=YESRAM DQ R<12>61 68 69</div><div>NO TEST=YESRAM DQ R<11>61 68 69</div></div>	<div><div>EE IDENTIFIED NO TEST NETS</div><div>NO TEST=YESNC EI NB TO CPU B CLK P56</div><div>NO TEST=YESNC EI NB TO CPU B CLK N56</div><div>NO TEST=YESNC EI NB TO CPU B AD<0..43>56</div><div>NO TEST=YESNC EI NB TO CPU B SR P<0..1>56</div><div>NO TEST=YESNC EI NB TO CPU B SR N<0..1>56</div><div>NO TEST=YESNC EI CPU B TO NB CLK P56</div><div>NO TEST=YESNC EI CPU B TO NB CLK N56</div><div>NO TEST=YESNC EI CPU B TO NB AD<0..43>56</div><div>NO TEST=YESNC EI CPU B TO NB SR P<0..1>56</div><div>NO TEST=YESNC EI CPU B TO NB SR N<0..1>56</div><div>NO TEST=YESNC NB CPU A1 INT L56</div><div>NO TEST=YESNC NB CPU B0 INT L56</div><div>NO TEST=YESNC NB CPU B1 INT L56</div><div>NO TEST=YESNC CPU A1 OACK L56</div><div>NO TEST=YESNC CPU B0 OACK L56</div><div>NO TEST=YESNC CPU B1 OACK L56</div><div>NO TEST=YESNC HT MB TO NB CAD P<8..15>101</div><div>NO TEST=YESNC HT MB TO NB CAD N<8..15>101</div><div>NO TEST=YESNC HT NB TO MB CAD P<8..15>101</div><div>NO TEST=YESNC HT NB TO MB CAD N<8..15>101</div><div>NO TEST=YESNC CLK RAI 200M N<0>27</div><div>NO TEST=YESNC CLK RAI 200M P<0>27</div><div>NO TEST=YESNC CLK RAI PCIEA N<0>27</div><div>NO TEST=YESNC CLK RAI PCIEA P<0>27</div><div>NO TEST=YESNC CLK RAI PCIEB N<0>27</div><div>NO TEST=YESNC CLK RAI PCIEB P<0>27</div><div>NO TEST=YESNC CLK RAI PCIEC N<0>27</div><div>NO TEST=YESNC CLK RAI PCIEC P<0>27</div><div>NO TEST=YESNC A AVREG 082</div><div>NO TEST=YESNC A AVREG 182</div><div>NO TEST=YESNC A AVREG 282</div><div>NO TEST=YESNC CPU B APSYNC82</div><div>NO TEST=YESNC EI CPU B SYSCLK N27</div><div>NO TEST=YESNC EI CPU B SYSCLK P27</div><div>NO TEST=YESNC HT NB TO MB CLK N<1>101</div><div>NO TEST=YESNC HT NB TO MB CLK P<1>101</div><div>NO TEST=YESNC J2904 1129</div><div>NO TEST=YESNC J2904 1229</div><div>NO TEST=YESNC NCV1009 155</div><div>NO TEST=YESNC NCV1009 255</div><div>NO TEST=YESNC NCV1009 355</div><div>NO TEST=YESNC NCV1009 455</div><div>NO TEST=YESNC NCV1009 555</div><div>NO TEST=YESNC NCV1009 ADJ55</div><div>NO TEST=YESNC RAM ARB0 REF25MHZ27</div><div>NO TEST=YESNC RAM ARB1 REF25MHZ27</div><div>NO TEST=YESNC SMU PWRSEQ P1 088 89</div><div>NO TEST=YESNC SMU PWRSEQ P1 44</div><div>NO TEST=YESRFBDC38>88 89</div><div>NO TEST=YESRFBDC37>88 89</div><div>NO TEST=YESRFBDC36>88 89</div><div>NO TEST=YESRFBDC34>88 89</div><div>NO TEST=YESRFBDC33>88 89</div><div>NO TEST=YESRFBDC32>88 89</div><div>NO TEST=YESRFBDC31>88 89</div><div>NO TEST=YESRFBDC30>88 89</div><div>NO TEST=YESRFBDC28>88 89</div><div>NO TEST=YESRFBDC27>88 89</div><div>NO TEST=YESRFBDC26>88 89</div><div>NO TEST=YESRFBDC25>88 89</div><div>NO TEST=YESRFBDC23>88 89</div><div>NO TEST=YESRFBDC22>88 89</div><div>NO TEST=YESRFBDC21>88 89</div><div>NO TEST=YESRFBDC54>88 89</div><div>NO TEST=YESRFBDC53>88 89</div><div>NO TEST=YESRFBDC52>88 89</div><div>NO TEST=YESRFBDC50>88 89</div><div>NO TEST=YESRFBDC49>88 89</div><div>NO TEST=YESRFBDC48>88 89</div><div>NO TEST=YESRFBDC47>88 89</div><div>NO TEST=YESRFBDC45>88 89</div><div>NO TEST=YESRFBDC44>88 89</div><div>NO TEST=YESRFBDC42>88 89</div><div>NO TEST=YESRFBDC41>88 89</div><div>NO TEST=YESRFBDC40>88 89</div><div>NO TEST=YESRFBDC126>88 90</div><div>NO TEST=YESRFBDC125>88 90</div><div>NO TEST=YESRFBDC124>88 90</div><div>NO TEST=YESRFBDC122>88 90</div><div>NO TEST=YESRFBDC121>88 90</div><div>NO TEST=YESRFBDC120>88 90</div><div>NO TEST=YESRFBDC118>88 90</div><div>NO TEST=YESRFBDC117>88 90</div><div>NO TEST=YESRFBDC116>88 90</div><div>NO TEST=YESRFBDC114>88 90</div><div>NO TEST=YESRFBDC113>88 90</div><div>NO TEST=YESRFBDC112>88 90</div><div>NO TEST=YESRFBDC110>88 90</div><div>NO TEST=YESRFBDC109>88 90</div><div>NO TEST=YESRFBDC108>88 90</div><div>NO TEST=YESRFBDC106>88 90</div><div>NO TEST=YESRFBDC105>88 90</div><div>NO TEST=YESRFBDC104>88 90</div><div>NO TEST=YESRFBDC102>88 90</div><div>NO TEST=YESRFBDC101>88 90</div><div>NO TEST=YESRFBDC100>88 90</div><div>NO TEST=YESRFBDC98>88 90</div><div>NO TEST=YESRFBDC97>88 90</div><div>NO TEST=YESRFBDC96>88 90</div><div>NO TEST=YESRFBDC95>88 90</div><div>NO TEST=YESRFBDC94>88 90</div><div>NO TEST=YESRFBDC92>88 90</div><div>NO TEST=YESRFBDC91>88 90</div><div>NO TEST=YESRFBDC90>88 90</div><div>NO TEST=YESRFBDC88>88 90</div><div>NO TEST=YESRFBDC87>88 90</div><div>NO TEST=YESRFBDC86>88 90</div><div>NO TEST=YESRFBDC85>88 90</div><div>NO TEST=YESRFBDC83>88 90</div><div>NO TEST=YESRFBDC82>88 90</div><div>NO TEST=YESRFBDC81>88 90</div><div>NO TEST=YESRFBDC79>88 90</div><div>NO TEST=YESRFBDC78>88 90</div><div>NO TEST=YESRFBDC76>88 90</div><div>NO TEST=YESRFBDC75>88 90</div><div>NO TEST=YESRFBDC74>88 90</div><div>NO TEST=YESRFBDC72>88 90</div><div>NO TEST=YESRFBDC71>88 90</div><div>NO TEST=YESRFBDC70>88 90</div><div>NO TEST=YESRFBDC69>88 90</div><div>NO TEST=YESRFBDC67>88 90</div><div>NO TEST=YESRFBDC66>88 90</div><div>NO TEST=YESRFBDC65>88 90</div><div>NO TEST=YESRFBDC62>88 90</div></div>	<div><div>FUNC TEST NETS</div><div>NOTES FROM TOM FUSSELMAN</div><div>PLACE TWO TEST POINTS ON TOP SIDE FOR PP3V3_ALL AND GND</div><div>PLACE WITHIN 1 INCH OF EACH OTHER</div><div>USE FAT TRACES</div><div>TOP SIDE ONLY</div><div>FUNC TEST=TRUESMU BOOT SCLK28 29</div><div>FUNC TEST=TRUESMU BOOT RXD28 29</div><div>FUNC TEST=TRUESMU BOOT CE28 29</div><div>FUNC TEST=TRUESMU BOOT CNVSS28 29</div><div>FUNC TEST=TRUESMU BOOT TXD28 29</div><div>FUNC TEST=TRUESMU BOOT BUSY28 29</div><div>FUNC TEST=TRUESMU MANUAL RESET L29</div><div>PP1V2_ALL FUNC TEST=TRUE</div><div>PP3V3_ALL FUNC TEST=TRUE</div><div>PP5V_ALL</div><div>PP1V8_RUN FUNC TEST=TRUE</div><div>PP2V5_RUN FUNC TEST=TRUE</div><div>PP3V3_RUN FUNC TEST=TRUE</div><div>PP12V_RUN</div><div>PP1V5_PWRON FUNC TEST=TRUE</div><div>GND FUNC TEST=TRUE</div><div>FUNC TEST 1 OF 2</div><div>SYNC_MASTER=FINO-ME</div><div>SYNC_DATE=06/20/2005</div><div>NOTICE OF PROPRIETARY PROPERTY</div><div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. 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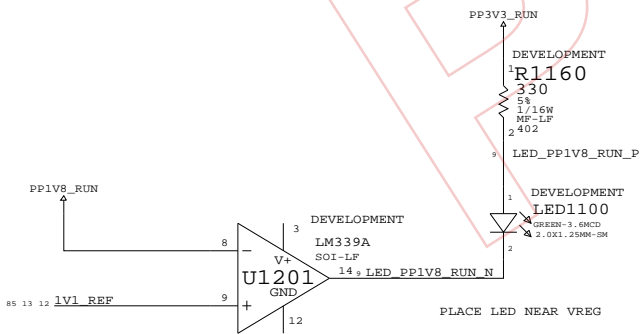
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	7 OF 154
NONE			

8	7	6	5	4	3	2	1
D	THE FOLLOWING NETS ARE USED ONLY WHEN THE DEVELOPMENT BOM OPTION IS ENABLED		THE FOLLOWING NETS DO NOT HAVE TEST POINT BECAUSE OF ROUTING DENSITY AND SIGNAL INTEGRITY. TEST COVERAGE WILL BE BY FCT NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS		JTAG TEST POINTS NEED TO BE ON THE BOTTOM OF THE BOARD ADDING FUNC_TEST=TRUE TO THESE NETS		
	NO_TEST=YES	ENET_TXD_R<7>	130 131	NO_TEST=YES	TP_VESTA_TVCO_24	139	
	NO_TEST=YES	ENET_TXD_R<6>	130 131	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132	
	NO_TEST=YES	ENET_TXD_R<5>	130 131	NO_TEST=YES	TP_I2S2_SB_TO_DEV.DTO	154	
	NO_TEST=YES	ENET_TXD_R<4>	130 131	NO_TEST=YES	TP_NB_APSYNC	44	
	NO_TEST=YES	ENET_TXD_R<3>	130 131	NO_TEST=YES	TP_SB_WATCHDOG	24	
	NO_TEST=YES	ENET_TXD_R<2>	130 131	NO_TEST=YES	NC_CPU_TBN.CLK		
	NO_TEST=YES	ENET_TXD_R<1>	130 131	NO_TEST=YES	NC_J3108_10	31	
	NO_TEST=YES	ENET_TXD_R<0>	130 131	NO_TEST=YES	NC_J3108_11	31	
	NO_TEST=YES	ENET_TXD<7>	130 131 132	NO_TEST=YES	NC_J3108_12	31	
C	NO_TEST=YES	ENET_TXD<6>	130 131 132	NO_TEST=YES	NC_J3108_8	31	
	NO_TEST=YES	ENET_TXD<5>	130 131 132	NO_TEST=YES	NC_J3108_9	31	
	NO_TEST=YES	ENET_TXD<4>	130 131 132	NO_TEST=YES	NC_JTAGMUX_3	30	
	NO_TEST=YES	ENET_TXD<3>	130 131 132	NO_TEST=YES	NC_PPIV5_PULSAR	12	
	NO_TEST=YES	ENET_TXD<2>	130 131 132				
	NO_TEST=YES	ENET_TXD<1>	130 131 132				
	NO_TEST=YES	ENET_TXD<0>	130 131 132				
	NO_TEST=YES	ENET_RXD_R<7>	130 131 132				
	NO_TEST=YES	ENET_RXD_R<6>	130 131 132				
	NO_TEST=YES	ENET_RXD_R<5>	130 131 132				
B	NO_TEST=YES	ENET_RXD_R<4>	130 131 132				
	NO_TEST=YES	ENET_RXD_R<3>	130 131 132				
	NO_TEST=YES	ENET_RXD_R<2>	130 131 132				
	NO_TEST=YES	ENET_RXD_R<1>	130 131 132				
	NO_TEST=YES	ENET_RXD_R<0>	130 131 132				
	NO_TEST=YES	ENET_RXD<7>	130 131				
	NO_TEST=YES	ENET_RXD<6>	130 131				
	NO_TEST=YES	ENET_RXD<5>	130 131				
	NO_TEST=YES	ENET_RXD<4>	130 131				
	NO_TEST=YES	ENET_RXD<3>	130 131				
A	NO_TEST=YES	ENET_RXD<2>	130 131				
	NO_TEST=YES	ENET_RXD<1>	130 131				
	NO_TEST=YES	ENET_RXD<0>	130 131				
	NO_TEST=YES	ENET_TX_EN_R	130 131				
	NO_TEST=YES	ENET_TX_ER_R	130 131				
	NO_TEST=YES	ENET_TX_EN	130 131 132				
	NO_TEST=YES	ENET_TX_ER	130 131 132				
	NO_TEST=YES	TP_HT_MB_TO_NB.CLK_N<1>	101				
	NO_TEST=YES	TP_HT_MB_TO_NB.CLK_P<1>	101				
	NO_TEST=YES	NC_CPU_AFN	56				
THE FOLLOWING PULSAR NETS WILL BE TESTED VIA TEST JET							
NO_TEST=YES	CPU_A_TBN.CLK_R	26					
NO_TEST=YES	CPU_B_TBN.CLK_R	26					
NO_TEST=YES	CPU_A_APSYNC_R	26					
NO_TEST=YES	CPU_B_APSYNC_R	26					
NO_TEST=YES	NB_APSYNC_R	26					
NO_TEST=YES	HT_SB_REFCLK_R	26					
NO_TEST=YES	HT_NB_REFCLK_H0_R	26					
NO_TEST=YES	HT_NB_REFCLK_L0_R	26					
NO_TEST=YES	CLK_RAIREF_200M_P_R	26					
NO_TEST=YES	CLK_RAIREF_200M_N_R	26					
NO_TEST=YES	NB_PMR.CLK_P_R	26					
NO_TEST=YES	NB_PMR.CLK_N_R	26					
NO_TEST=YES	NB_PCIE_REFCLK_P_C	26					
NO_TEST=YES	NB_PCIE_REFCLK_N_C	26					
NO_TEST=YES	GPU_DIODE_PLUS	93					
NO_TEST=YES	GPU_DIODE_MINUS	93					
NO_TEST=YES	LED8700_P	136					
NO_TEST=YES	LED8701_P	136					
ADDING NO_TEST TO ALL PCIE NETS TO AVOID STUBS WILL GET COVERAGE IN FCT WITH A DIAG THAT CHECKS THAT THE BUS IS 16 LANES WIDE							
NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<0..15>	9 82 97					
NO_TEST=YES	PCIE_NB_TO_SLOTA_P<0..15>	9 82 97					
NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0..15>	9 82 84 97					
NO_TEST=YES	PCIE_NB_TO_SLOTA_P<0..15>	9 82 84 97					
NO_TEST=YES	PCIE_SLOTA_TO_NB_NF<0..15>	84 97					
NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	84 97					
NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97					
NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97					
FUNG TEST 2 OF 2							
SYNC_MASTER=FINO-ME							
SYNC_DATE=06/20/2005							
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APPLE COMPUTER INC.							
SIZE	D	DRAWING NUMBER	051-6790	REV.	19		
SCALE	NONE	SHT	9	OF	154		

1.8V VOLTAGE REGULATOR

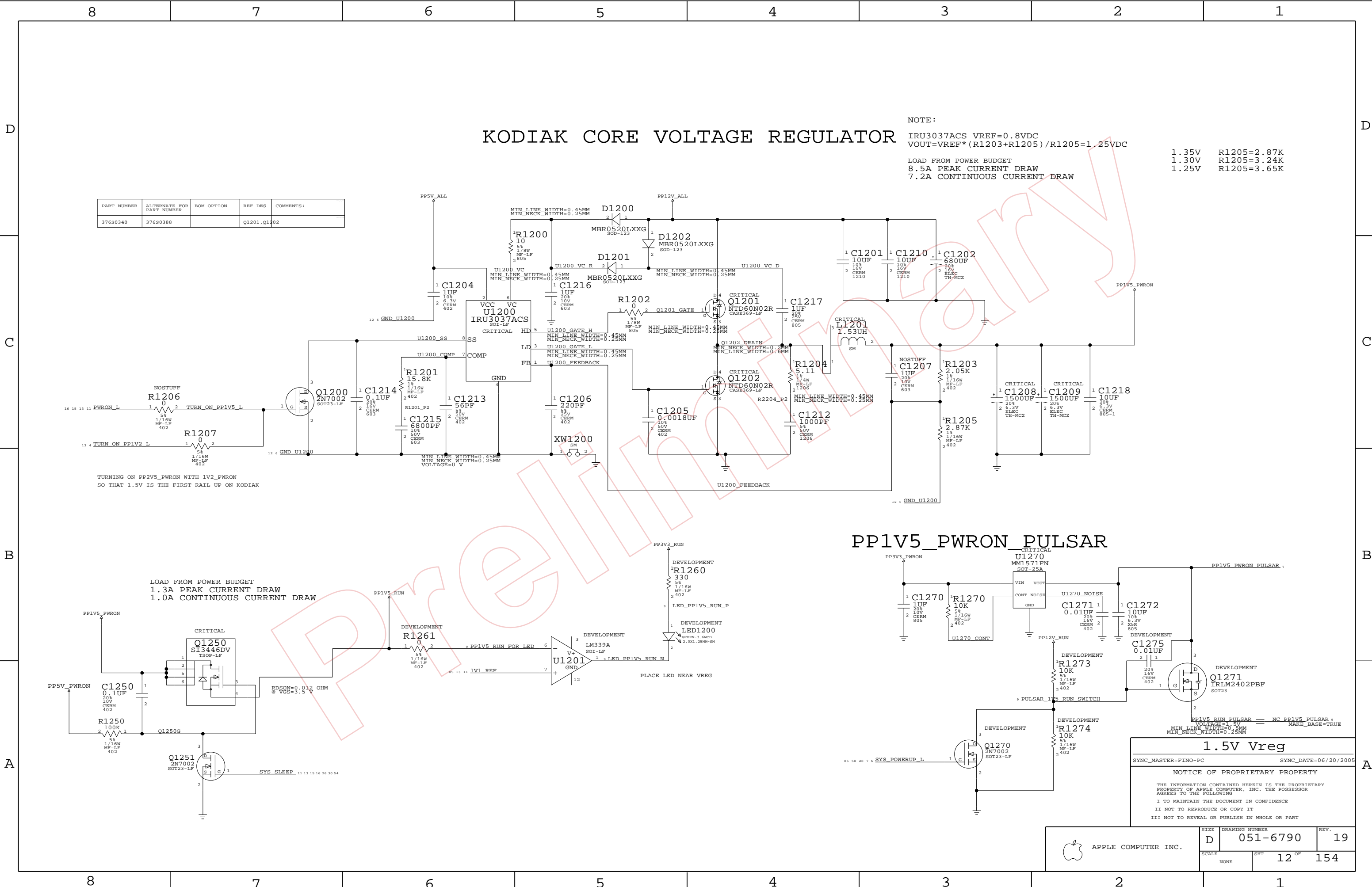


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1101,Q1102	

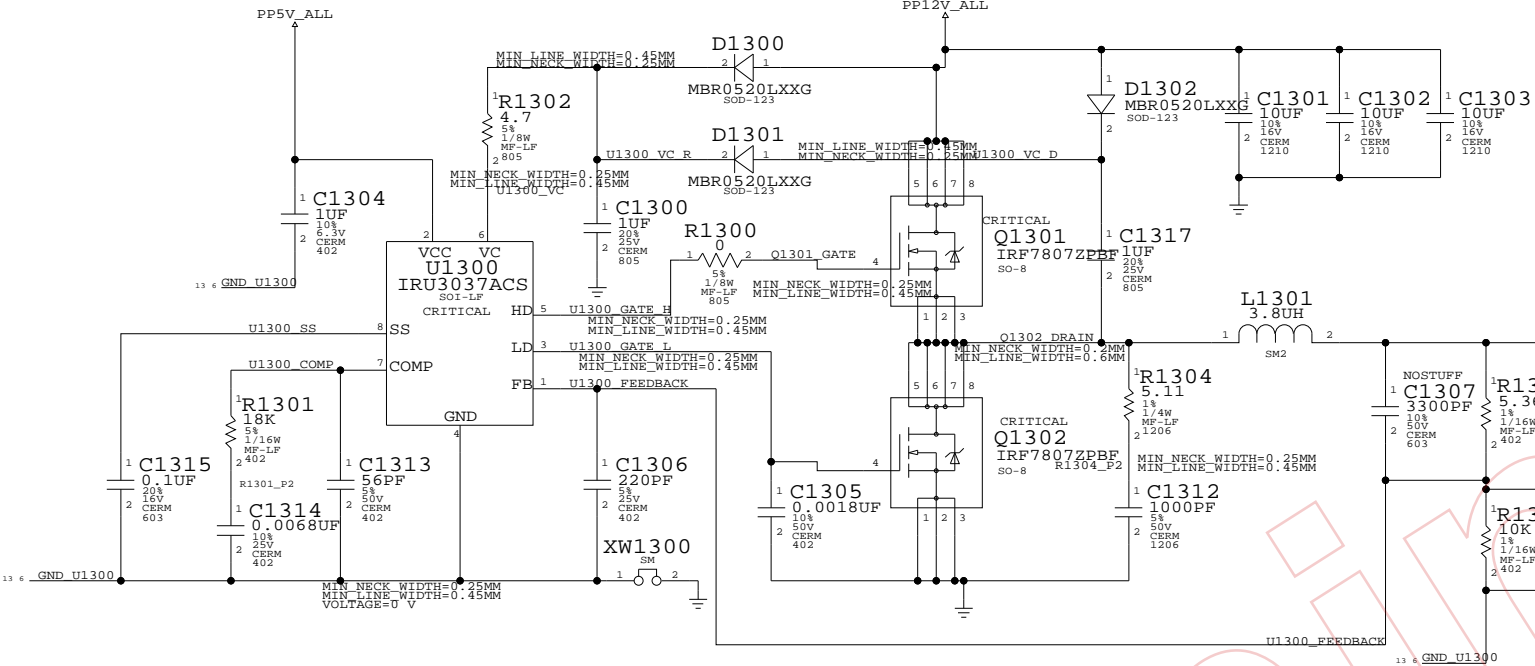


1.8V Vreg	
SYNC_MASTER=M23-PC	SYNC_DATE=06/20/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	11 OF 154
NONE			



PP1V2_ALL VOLTAGE REGULATOR

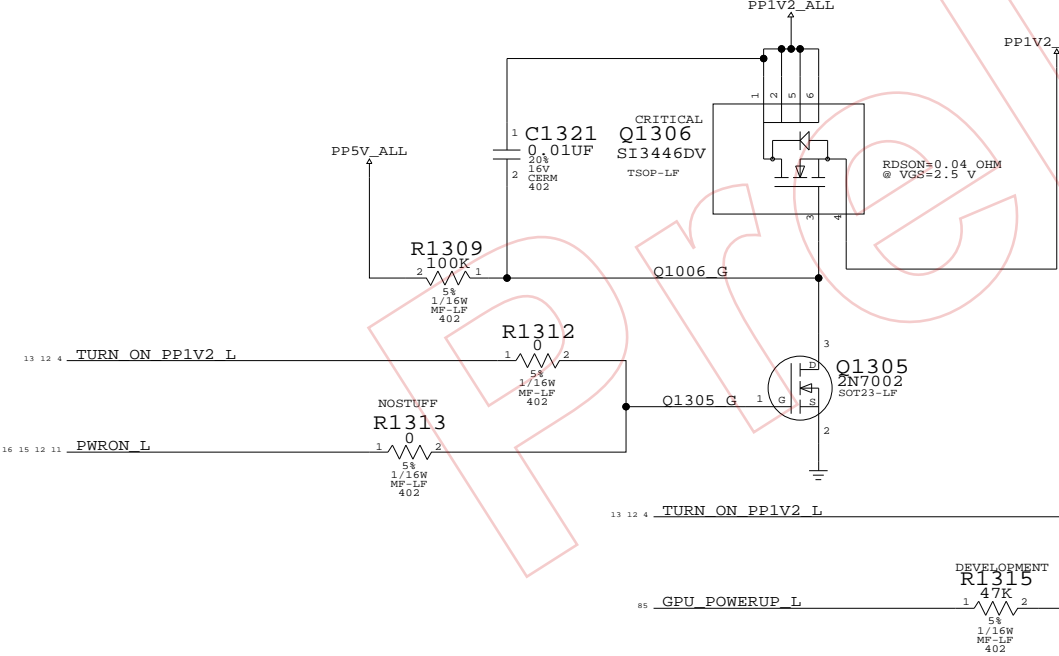


NOTE:
SET OUTPUT=1.22-1.23V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC

POWER BUDGET CURRENT OF TOTAL RAILS
3.2A PEAK
2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

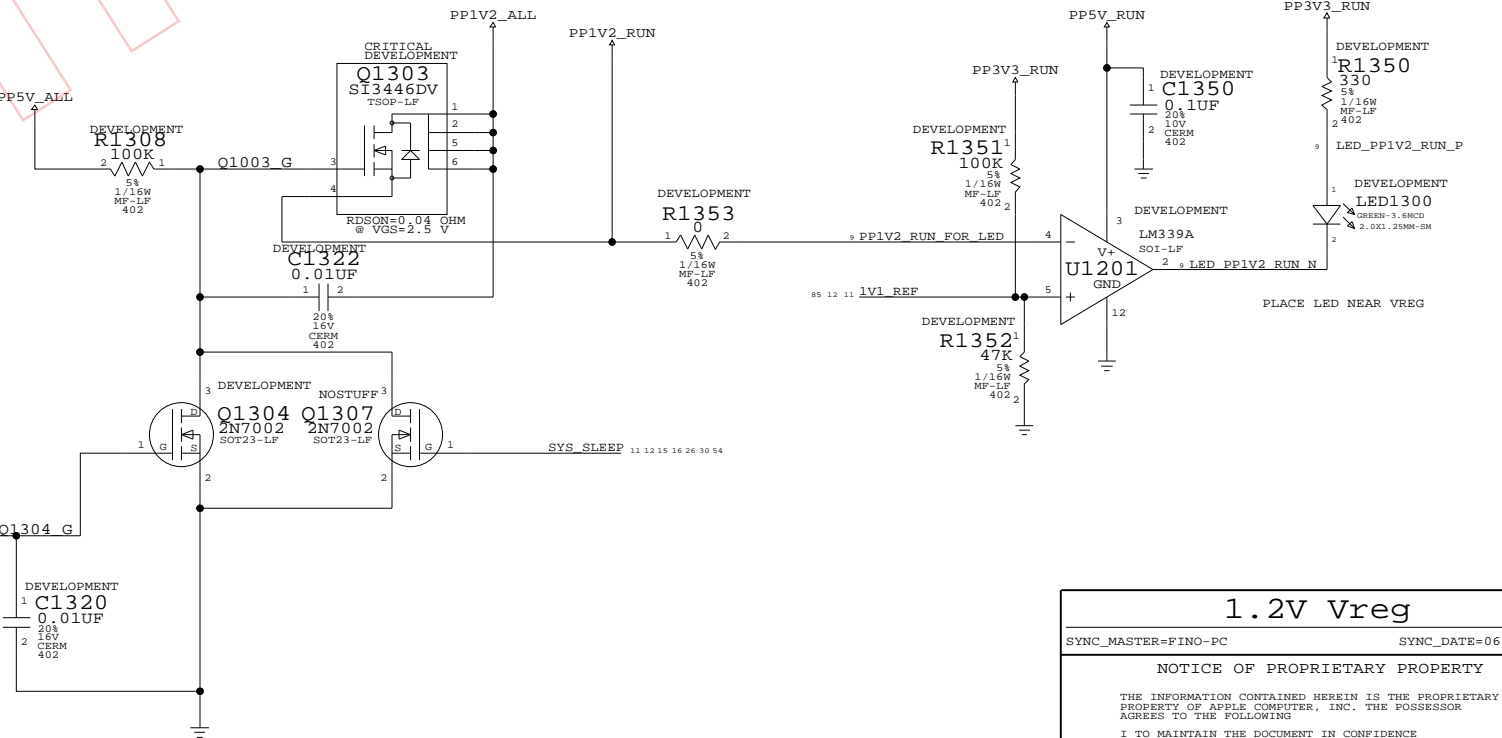
PEAK CURRENT 1.3A
1.0A CONTINUOUS



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



1.2V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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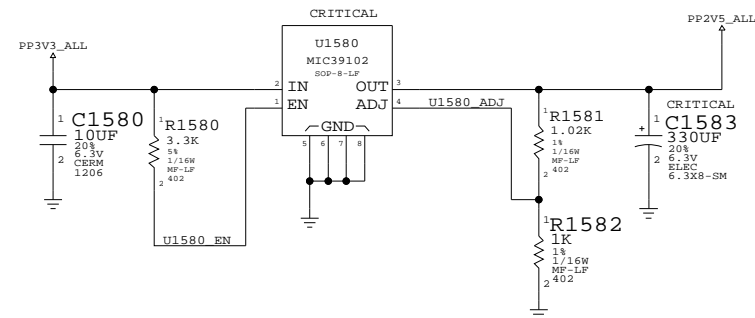
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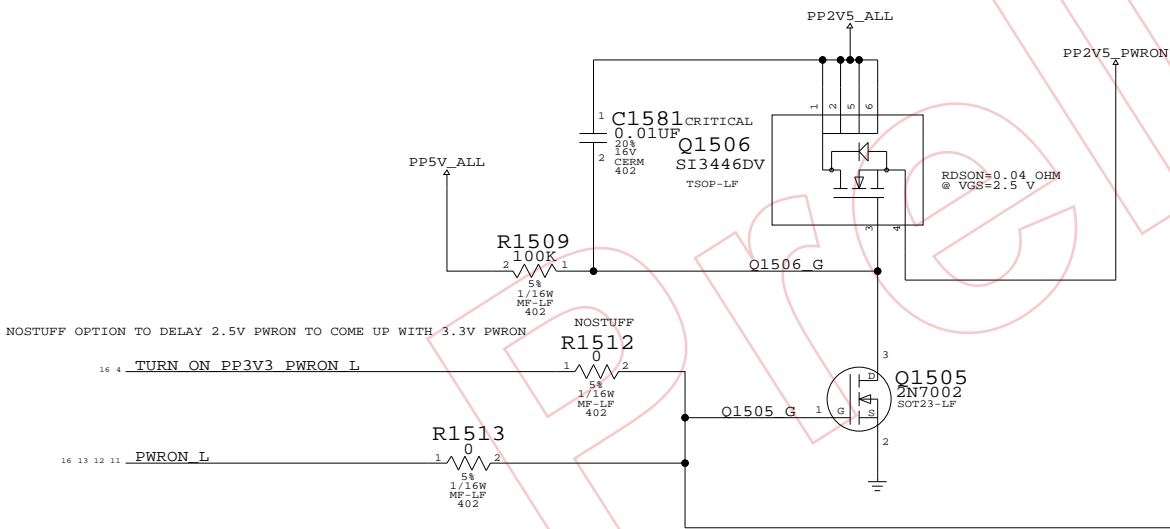
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
	SCALE	SHT	13 OF 154
	NONE		

PP2V5_ALL VOLTAGE REGULATOR

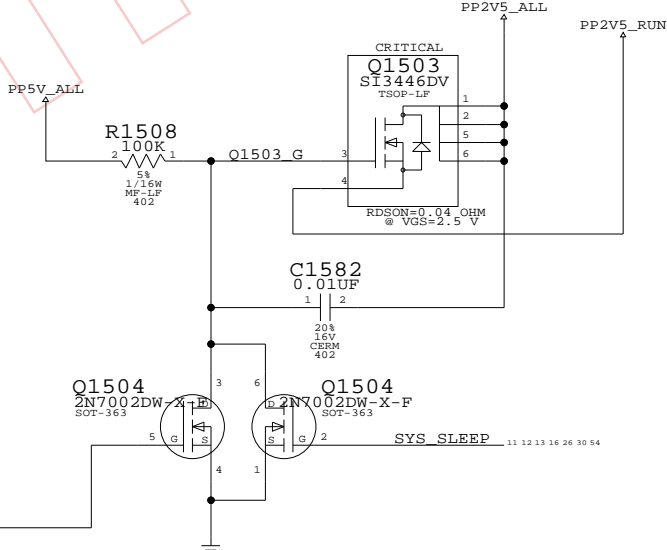


NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
 $V_{OUT}=V_{REF} \cdot (R1581+R1582)+1=5.505VDC$
POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

PP2V5_PWRON FET SWITCH
PEAK CURRENT 0.1A



PP2V5_RUN FET SWITCH
PEAK CURRENT 0.1A



2.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

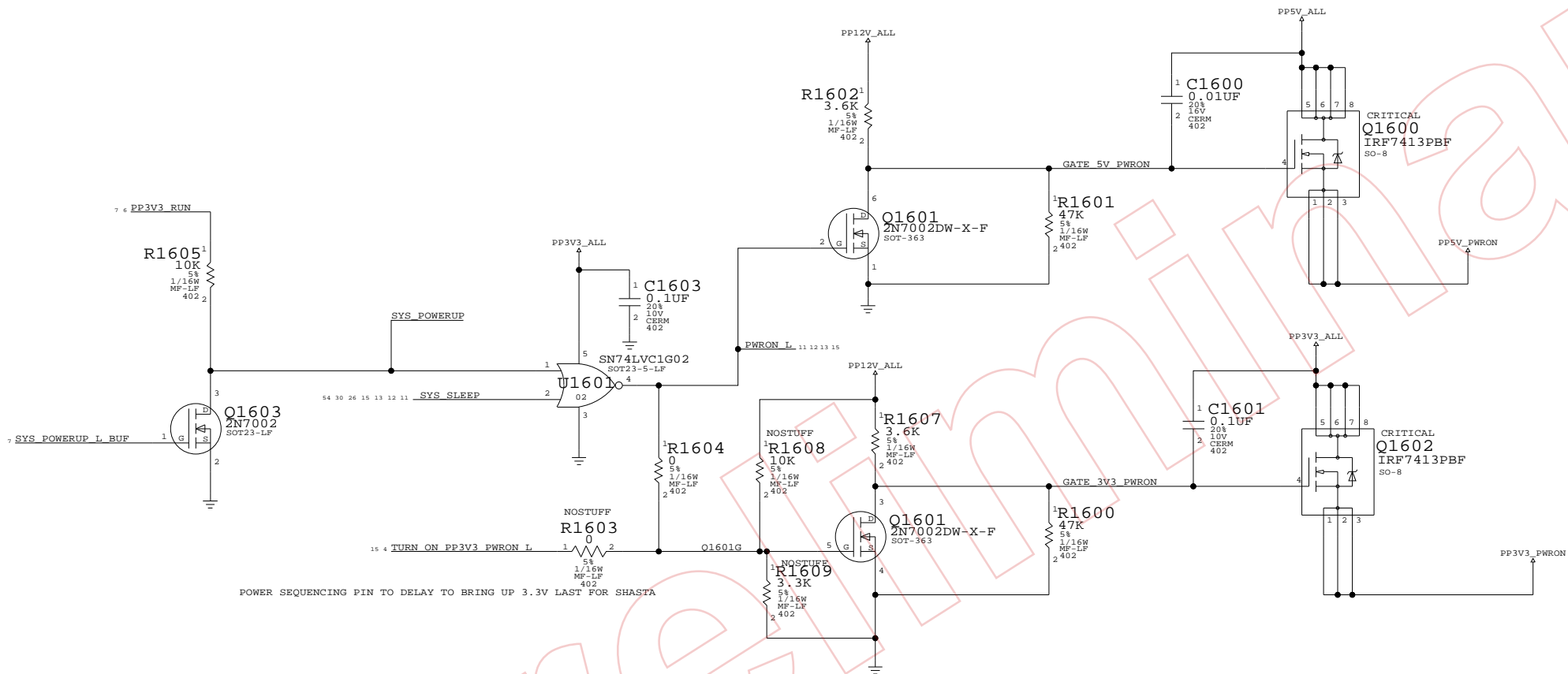
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	D	051-6790	19
SCALE		SHT	15 OF 154
NONE			



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	19
SCALE	SHT	16 OF 154
NONE		

Page Notes

Power aliases required by this page:

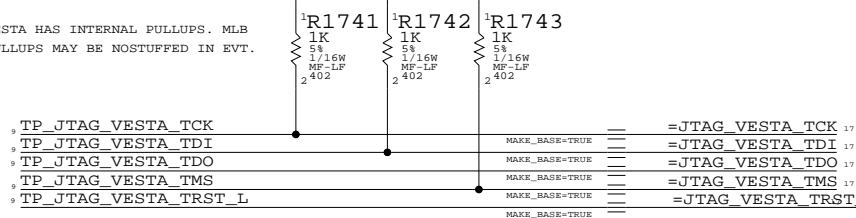
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG

139 132 17 7 =PP3V3_ENETFW

VESTA HAS INTERNAL PULLUPS. MLB
PULLUPS MAY BE NOSTUFFED IN EVT.



TP_JTAG_VESTA_TCK
TP_JTAG_VESTA_TDI
TP_JTAG_VESTA_TDO
TP_JTAG_VESTA_TMS
TP_JTAG_VESTA_TRST_L

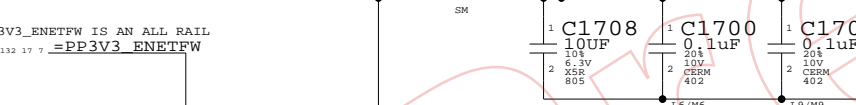
MAKE_BASE=TRUE
MAKE_BASE=TRUE
MAKE_BASE=TRUE
MAKE_BASE=TRUE
MAKE_BASE=TRUE

=JTAG_VESTA_TCK 17
=JTAG_VESTA_TDI 17
=JTAG_VESTA_TDO 17
=JTAG_VESTA_TMS 17
=JTAG_VESTA_TRST_L



L1700
FERR-EMI-600-OHM
MIN_LINK_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.2V

PP1V2_VESTA_AVDDL

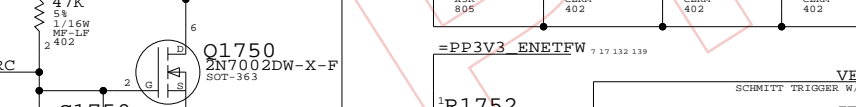


M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1750
10K 5% 1/16W MF-LP 402

R1751
47K 5% 1/16W MF-LP 402

C1750
10uF 10V CERM 402



VESTA RESET RC

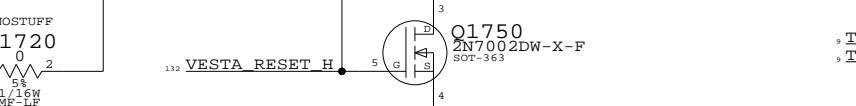
Q1750
2N7002DW-X-F
SOT-363

PP3V3_ENETFW 7 17 132 139

R1752
10K 5% 1/16W MF-LP 402

RESET ASSERT REQUIREMENT IS 20MS TO 100MS

Q1750
2N7002DW-X-F
SOT-363



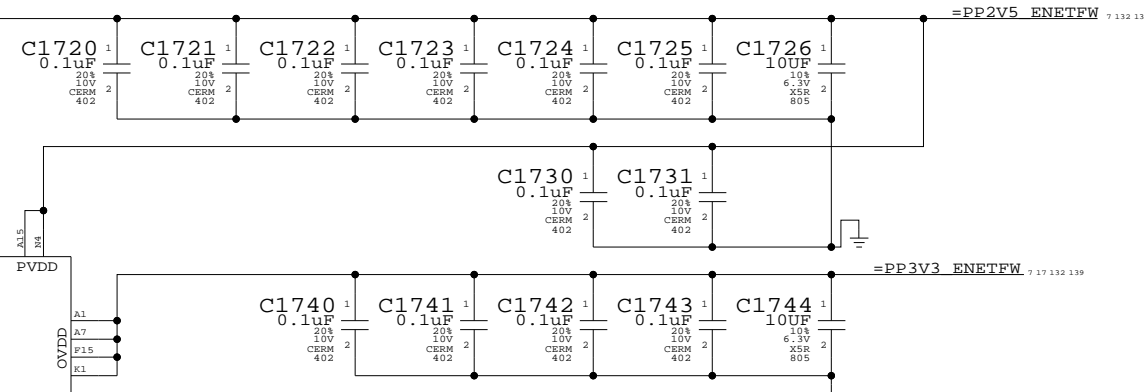
NOSTUFF
R1720
0 1/16W MF-LP 402

ENETFW_RESET 1 2

VESTA RESET H 132

To keep Vesta from being held
in reset when system is off
NOTE: Reset GPIO is active HIGH

M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS



2.5V_EN
0 - OVDD=3.3V
1 - OVDD=2.5V
WHEN OVDD=2.5V GMII PINS ARE NOT 3.3V TOLERANT

TP VESTA 2 5V EN

TP VESTA REGSUP1
TP VESTA REGSEN1
TP VESTA REGCTL1

TP VESTA REGSUP2
TP VESTA REGSEN2
TP VESTA REGCTL2

REGSUP1
REGSEN1
REGCTL1

REGSUP2
REGSEN2
REGCTL2

AGND
GND

Vesta Core / Misc

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	19
SCALE	SHT	OF
NONE	17	154

D

C

B

A

D

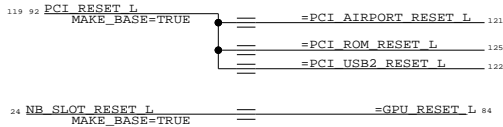
C

B

A

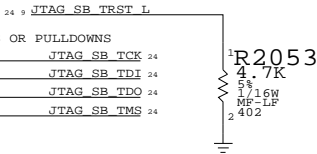
SHASTA ALIASES

PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)

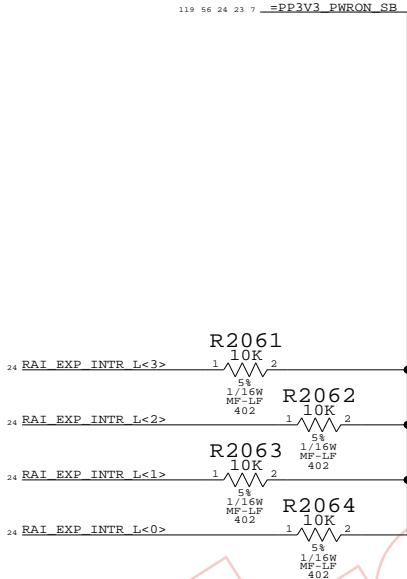


SHASTA JTAG

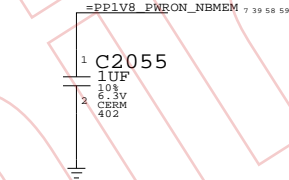
THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS
TP JTAG SB_TCK
MAKE_BASE=TRUE
TP JTAG SB_TDI
MAKE_BASE=TRUE
TP JTAG SB_TDO
MAKE_BASE=TRUE
TP JTAG SB_TMS
MAKE_BASE=TRUE



SHASTA GPIO TERMINATIONS
(SOME OF THESE ARE NOSTUFF
ON PAGE 24)

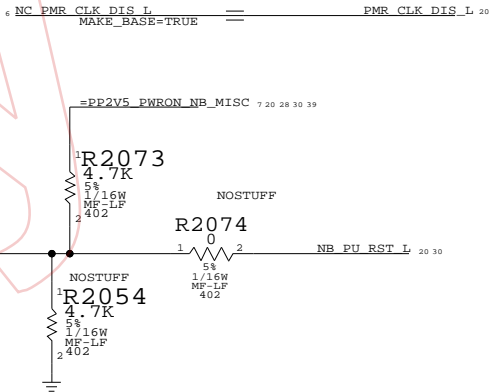


KODIAK JTAG_TRST PULLED HIGH
TO ALLOW SMU DEBUG ACCESS

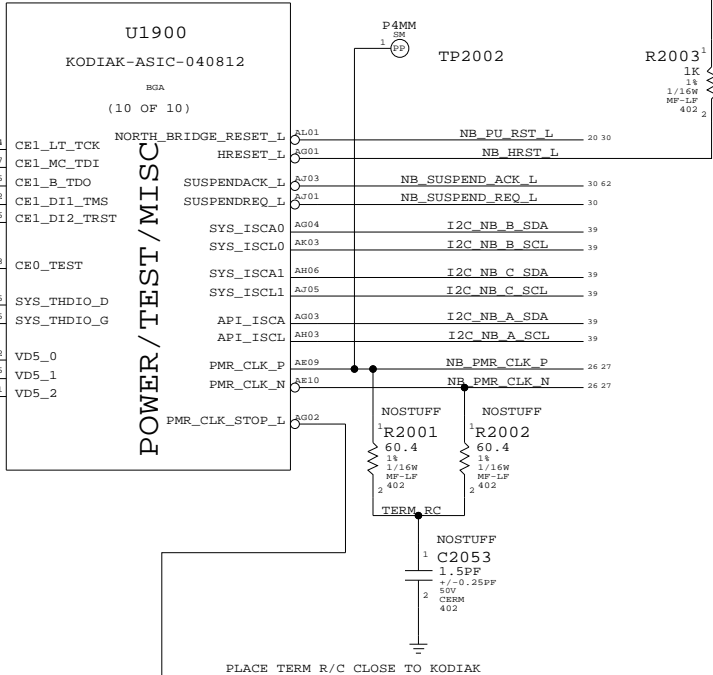


C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP

KODIAK ALIASES



POWER/TEST/MISC



KODIAK & SHASTA MISC

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	19
SCALE	SHT	OF
NONE	20	154

Page Notes

Power aliases required by this page:

```
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
```

```
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
```

- =PP3V3 PWRON SB

```
- =PF3V3_PWRON_SB
- =PR2M6_PWRON_SB
```

```
- #PP2V5_PWRON_SB
- #PP1V2_PWRON_SB VCORE
```

NOTE: PCI pads use the VIO supply to meet

different drive timing

characteristics required by the PCI

spec for 5V vs. 3.3V operation.

CONNECT VIO2 TO

appropriate PGT bus voltage and

VIO1 TO SAME IF 64-BIT

PCI, otherwise 3.3V.

Signal aliases required by this page:

(NONE)

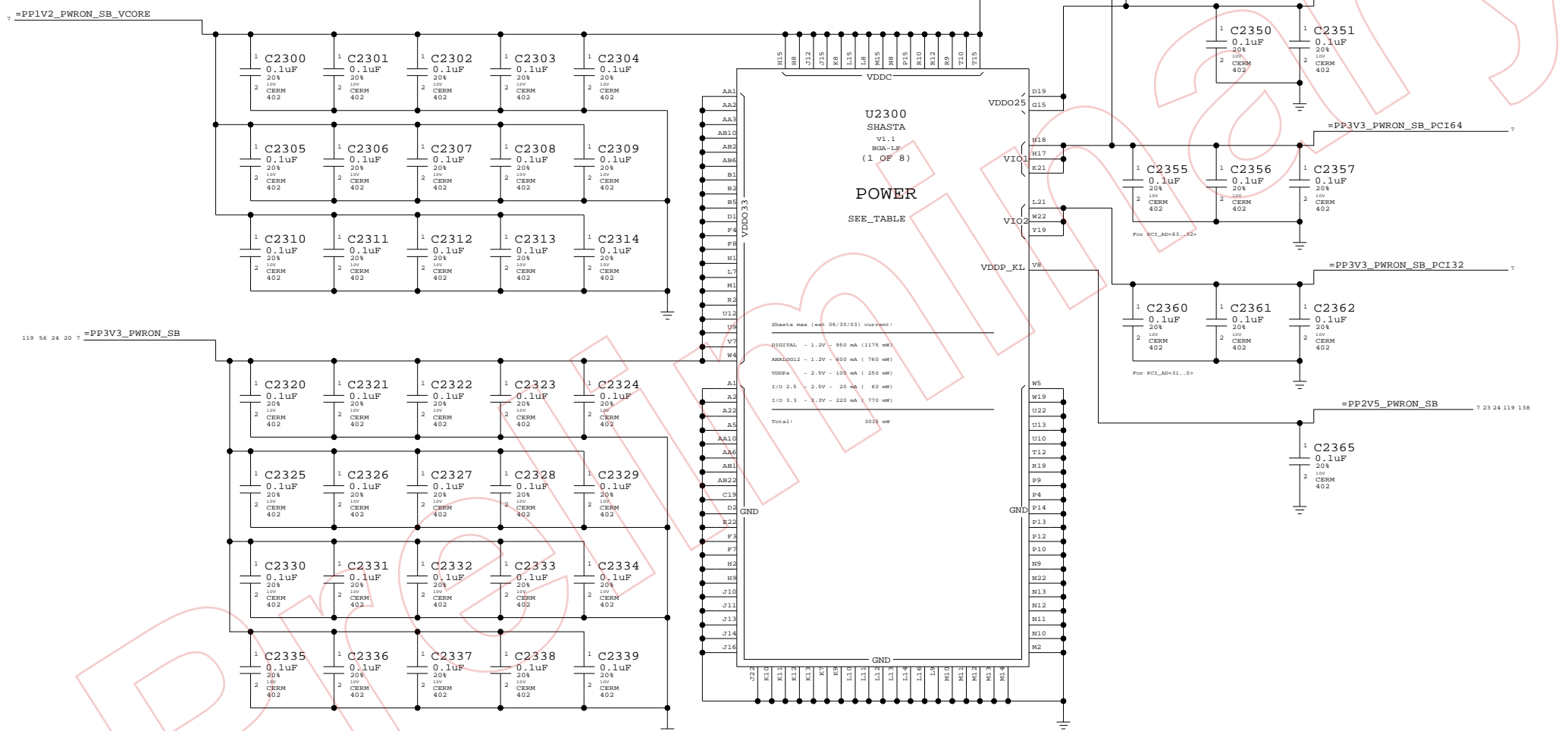
BOM options provided by this page:

(NONE)

Power Sequencing:

Must power Shasta VCore rail before any

other Shasta supplies.

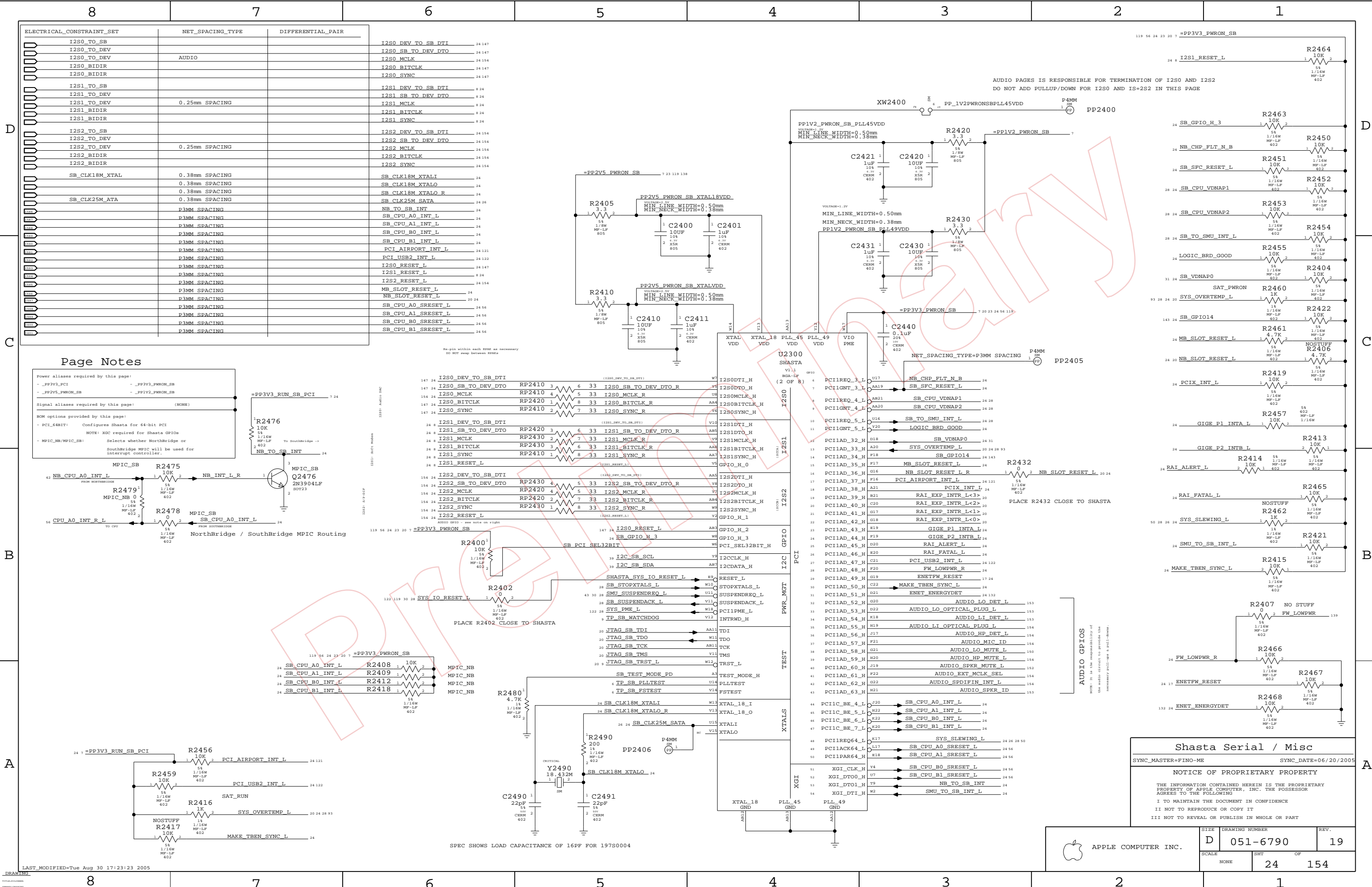


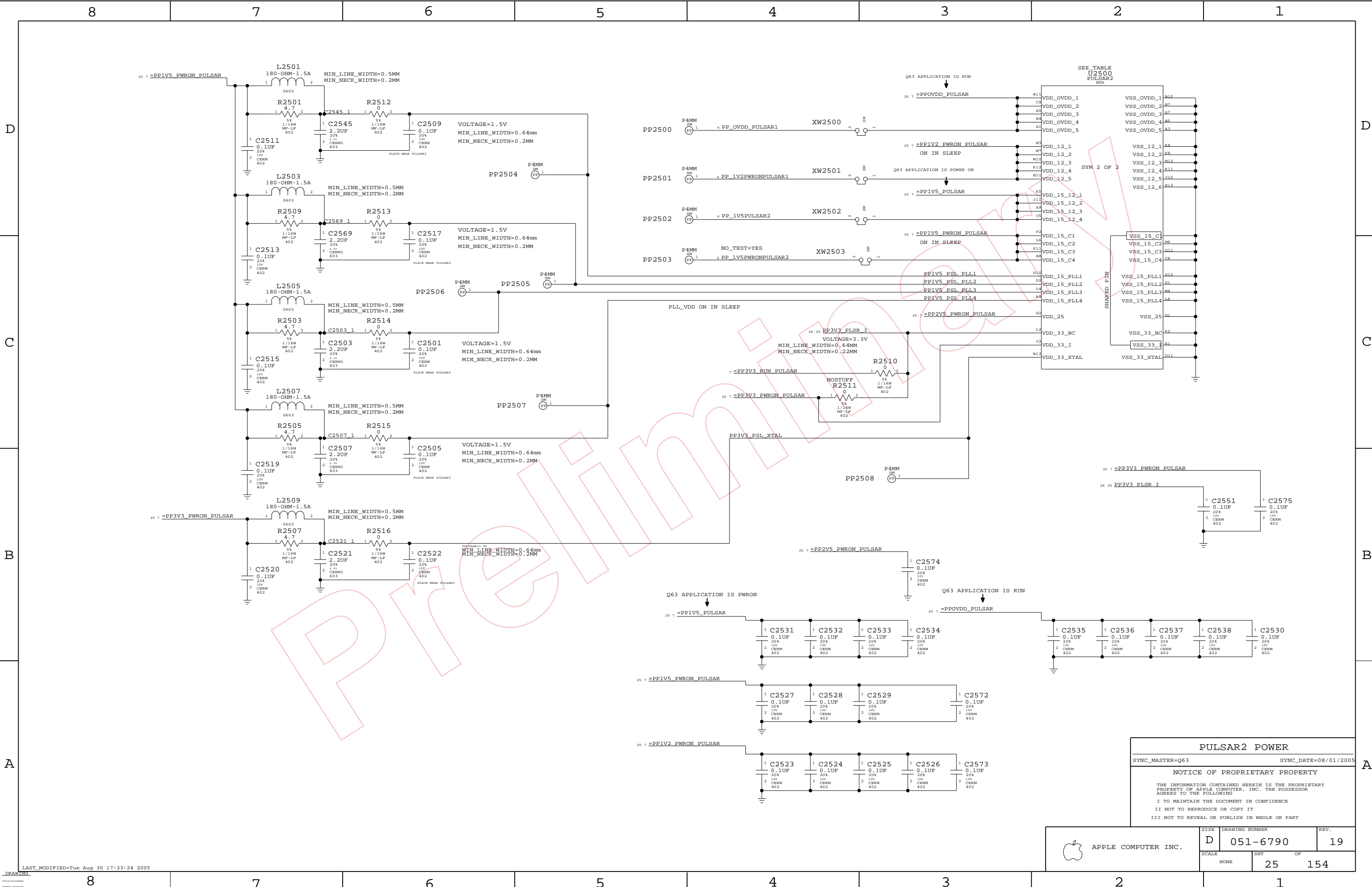
Shasta Core Power	
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005
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SIZE	DRAWING NUMBER	REV.
D	051-6790	19
SCALE	SHT	OF
NONE	23	154





LAST_MODIFIED= Tue Aug 30 17:23:24 2005

DRAWING

PULSAR2 POWER

SYNC_MASTER=Q63

SYNC_DATE=08/01/2005

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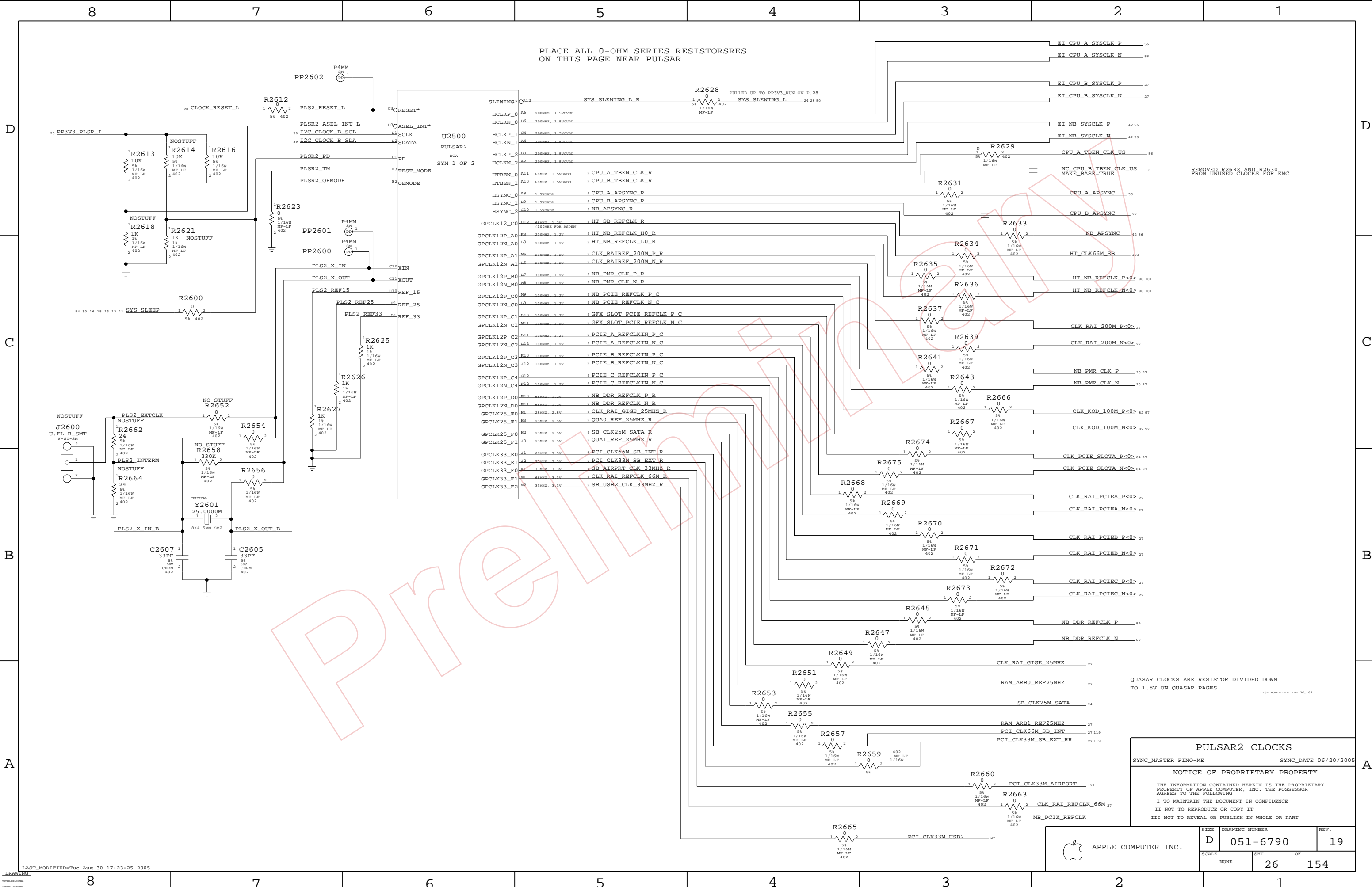
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	D	051-6790	19
SCALE	SHT		OF
	NONE	25	154





PLACE ALL 0-OHM SERIES RESISTORS
ON THIS PAGE NEAR PULSAR

REMOVED R2632 AND R2630
FROM UNUSED CLOCKS FOR EMC

QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES

LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS

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SIZE	DRAWING NUMBER	REV.
D	051-6790	19
SCALE	SHT	OF
NONE	26	154

D

D

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions require pull-ups that are not provided on this page. Please review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

C

C

B

B

A

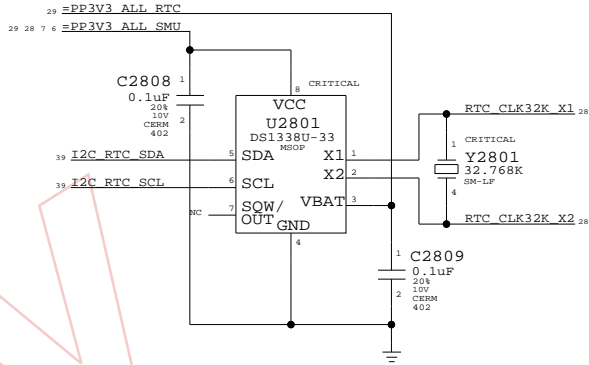
A

Alternate Functions

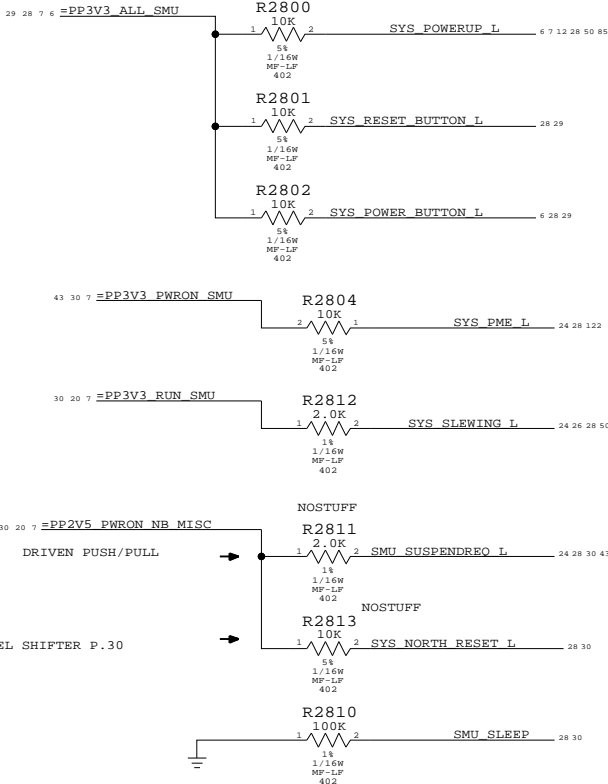
System Management Unit

Tower & Server			
Port		Port	
31 28 CPU VID<0>	6.0	SAT MRESET L	
31 28 CPU VID<1>	6.1	CPU A INSERTED L	
31 28 CPU VID<2>	6.2	CPU B INSERTED L	
31 28 I2C SMU CPU SDA IN	7.3	SMU FAN PWM8	
31 28 I2C SMU CPU SCL IN	7.4	SMU FAN PWM9	
31 28 I2C SMU A SDA IN	3.0	I2C SMU A SDA	31 39
31 28 I2C SMU A SDA OUT L	3.1	I2C SMU A SCL	31 39

Real Time Clock

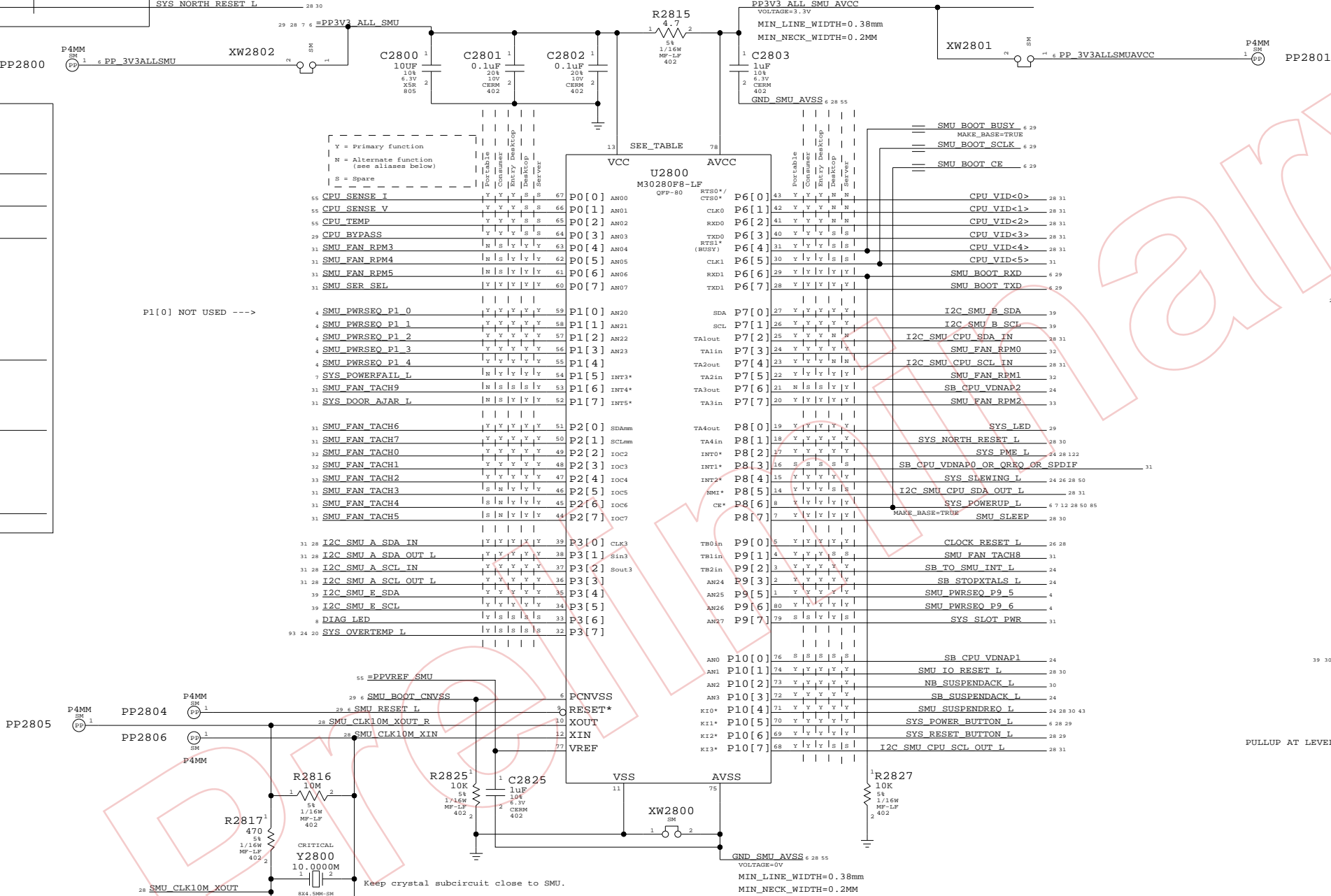


SMU Pull-ups / pull-down



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_CLK10M_XTAL	0.38MM SPACING	SMU_CLK10M_XIN
	0.38MM SPACING	SMU_CLK10M_XOUT
	0.38MM SPACING	SMU_CLK10M_XOUT_R
RTC_CLK32K_XTAL	0.38MM SPACING	RTC_CLK32K_X1
	0.38MM SPACING	RTC_CLK32K_X2
	P3MM SPACING	SMU_IO_RESET_L
	0.25MM SPACING	SYS_NORTH_RESET_L

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_RESET	0.25MM SPACING	SYS_NORTH_RESET_L
SMU_RESET	0.25MM SPACING	SYS_IO_RESET_L
	P3MM SPACING	CLOCK_RESET_L
	P3MM SPACING	SYS_RESET_BUTTON_L



System Management Unit

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

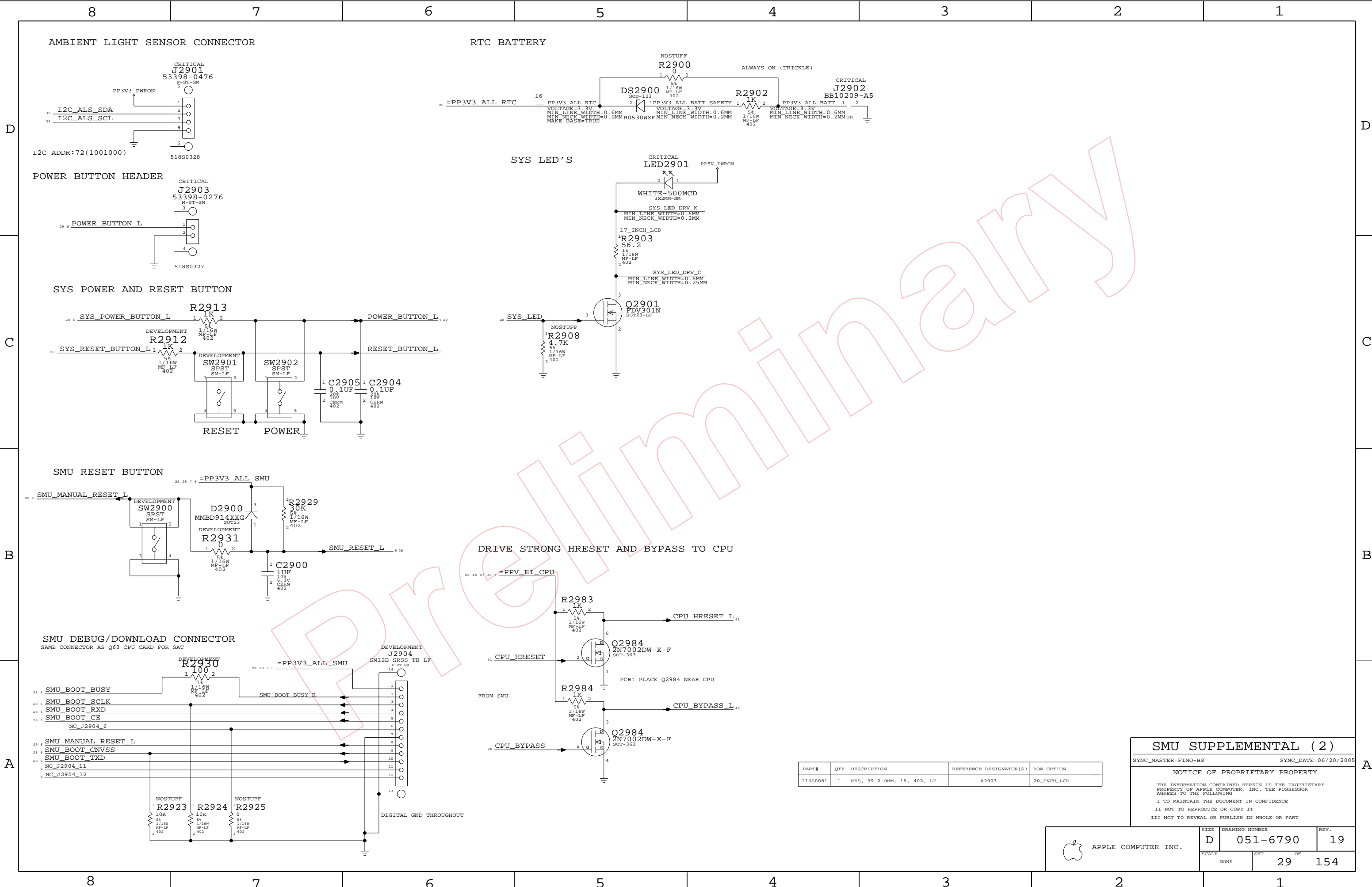
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D	051-6790	19
SCALE	SHT	OF
NONE	28	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES, 39.2 OHM, 1%, 402, LF	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

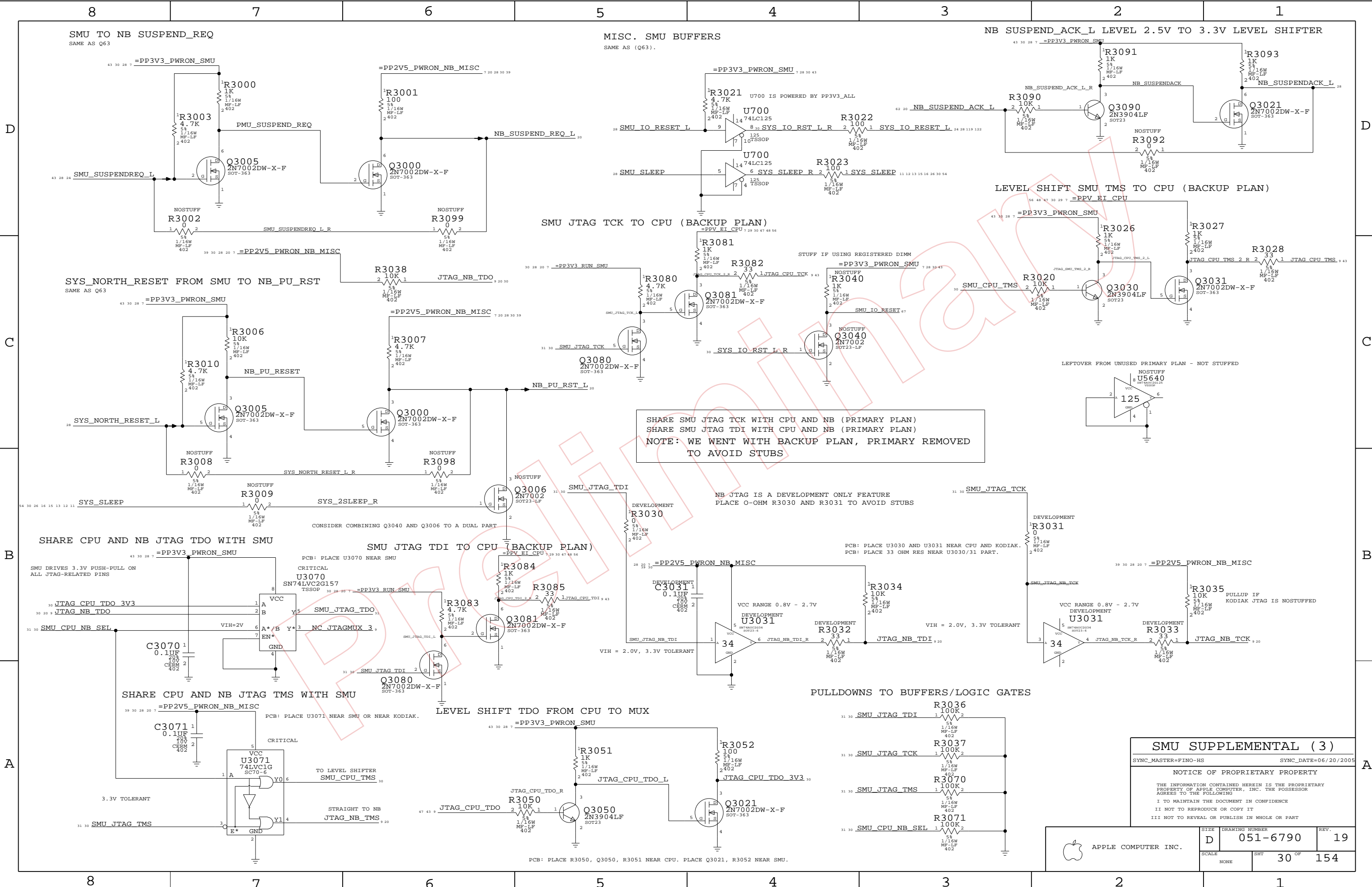
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
	SCALE	SHT	OF
	NONE	29	154



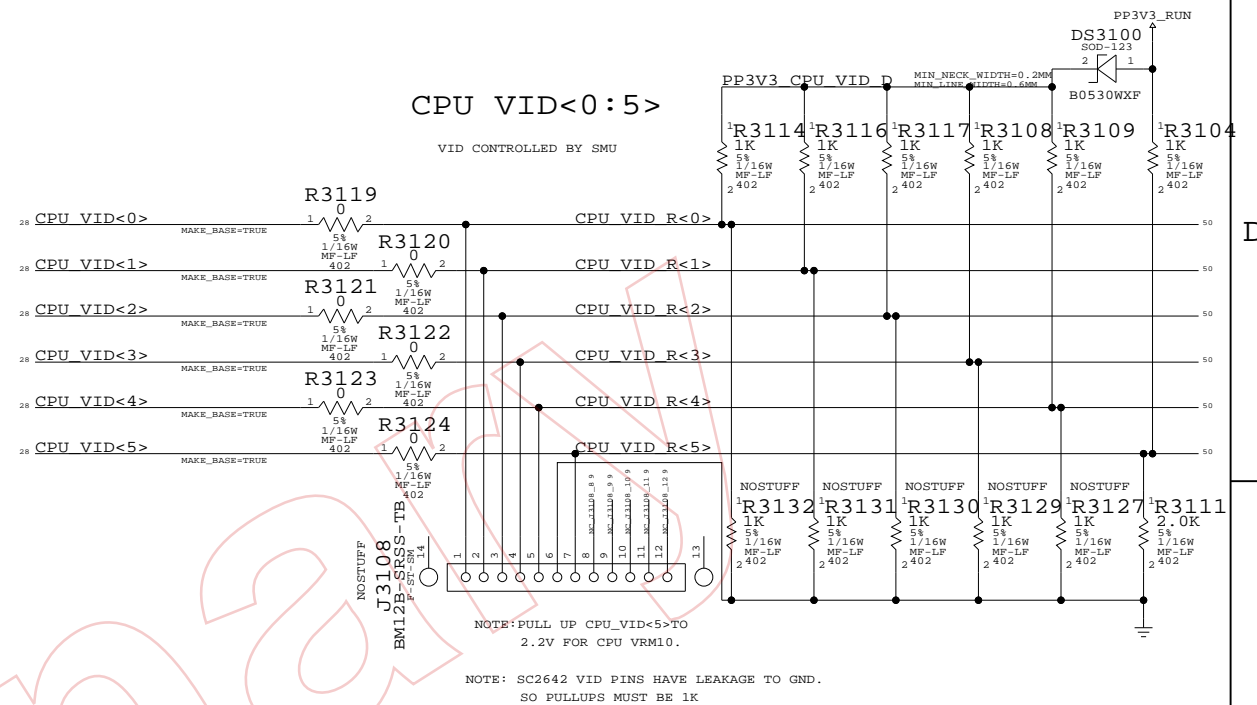
SMU SUPPLEMENTAL (3)		
SYNC_MASTER=FINO-HS		SYNC_DATE=06/20/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	30 OF 154
NONE			

SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION	Q63 NET NAME (SHARED PAGE)
	CPU_SENSE_I0	P0.0	
	CPU_SENSE_V0	P0.1	
	CPU_TEMP0	P0.2	
	CPU_BYPASS	P0.3	
Q63 NC'S THESE AS IT USES A SAT.			
	NC SMU FAN RPM3	FAN_CN1L0_4	SMU FAN RPM3
M23/M33 DOESN'T HAVE THOSE FANS.	NC SMU FAN RPM4	FAN_CN1L0_5	SMU FAN RPM4
	NC SMU FAN RPM5	FAN_CN1L0_6	SMU FAN RPM5
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	NC SMU SER SEL	SMU_SCC1_SEL	SMU SER SEL
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.			
	CPU_SENSE_I1	P1.0	
	CPU_SENSE_V1	P1.1	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.	CPU_TEMP1	P1.2	
	PS1_3	P1.3	
	PS1_4	P1.4	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.	POWERFAIL*	P1.5	
	NC SMU CPU VID LE0	CPH_VID_LE0	SMU FAN TACH9
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	NC SYS DOOR AJAR L	DOOR_AJAR*	SYS DOOR AJAR L
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	NC SMU CPU VID LE1	CPH_VID_LE1	SMU FAN TACH6
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	NC SMU FAN TACH7	FAN_TACH2_1	SMU FAN TACH7
M23/M33 DOESN'T HAVE THIS FAN.			
	FAN_TACH2_2	P2.2	
	FAN_TACH2_3	P2.3	
	FAN_TACH2_4	P2.4	
	NC SMU FAN TACH3	FAN_TACH2_5	SMU FAN TACH3
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	NC SMU FAN TACH4	FAN_TACH2_6	SMU FAN TACH4
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	NC SMU FAN TACH5	FAN_TACH2_7	SMU FAN TACH5
	I2C SMU A SDA	I1C_A_DAT*	I2C SMU A SDA IN
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	I2C SMU A SCL	I1C_A_CLK*	I2C SMU A SDA OUT L
	SMU JTAG TDI	TDI	I2C SMU A SCL IN
	SMU JTAG TCK	TCK	I2C SMU A SCL OUT L
	IIC_E_DAT	P3.4	
	IIC_E_CLK	P3.5	
	DIAG_LED	P3.6	
	OVERTEMP*	P3.7	
	CPU_VID[0]	P6.0	
	CPU_VID[1]	P6.1	
	CPU_VID[2]	P6.2	
	CPU_VID[3]	P6.3	
	CPU_VID[4]	P6.4	
	CPU_VID[5]	P6.5	
	DEBUG_RXD	P6.6	
	DEBUG_TXD	P6.7	
	IIC_B_DAT	P7.0	
	IIC_B_CLK	P7.1	
7.2 IS PWM FAN	SMU CPU NB SEL	CPH_TMS	I2C SMU CPU SDA IN
	NC I2C SMU CPU SCL IN	FAN_CN1L7_3	I2C SMU CPU SCL IN
M23/M33 DOESN'T HAVE THIS FAN (P7.4)			
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.			
	FAN_CN1L7_5	P7.5	
	VDNAP2	P7.6	
	FAN_CN1L7_7	P7.7	
	SYSTEM_LED	P8.0	
	NB_RESET*	P8.1	
	PME*	P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	SB VDNAP0	VDNAP0	SB CPU VDNAP0 OR QREQ OR SPDIF
	SMU JTAG TMS	SLEWING*	I2C SMU CPU SDA OUT L
	POWERUP*	P8.6	
	SLEEP	P8.7	
	CLK_RESET*	P9.0	
Q63 USE OF P9.1 IS TACH 8.	CPU HRESET	CPH_HRESET	SMU FAN TACH8
	SMU_DOORBELL*	P9.2	
	STOP_XTAL*	P9.3	
	PS9_5	P9.5	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.	PS9_6	P9.6	
M23/M33 HAS NO SLOTS.	NC SLOT TOTAL PWR	SLOT_TOTAL_PWR	SYS SLOT PWR
	VDNAP1	P10.0	
	IO_RESET*	P10.1	
	SUSPEND_ACK*	P10.2	
	SUSPEND_IO_ACK*	P10.3	
	SUSPEND_REQ*	P10.4	
	PWR_BUTTON*	P10.5	
	RST_BUTTON*	P10.6	
	SMU JTAG TDO	TDO	I2C SMU CPU SCL OUT L



SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-HS	SYNC_DATE=06/20/2005	7
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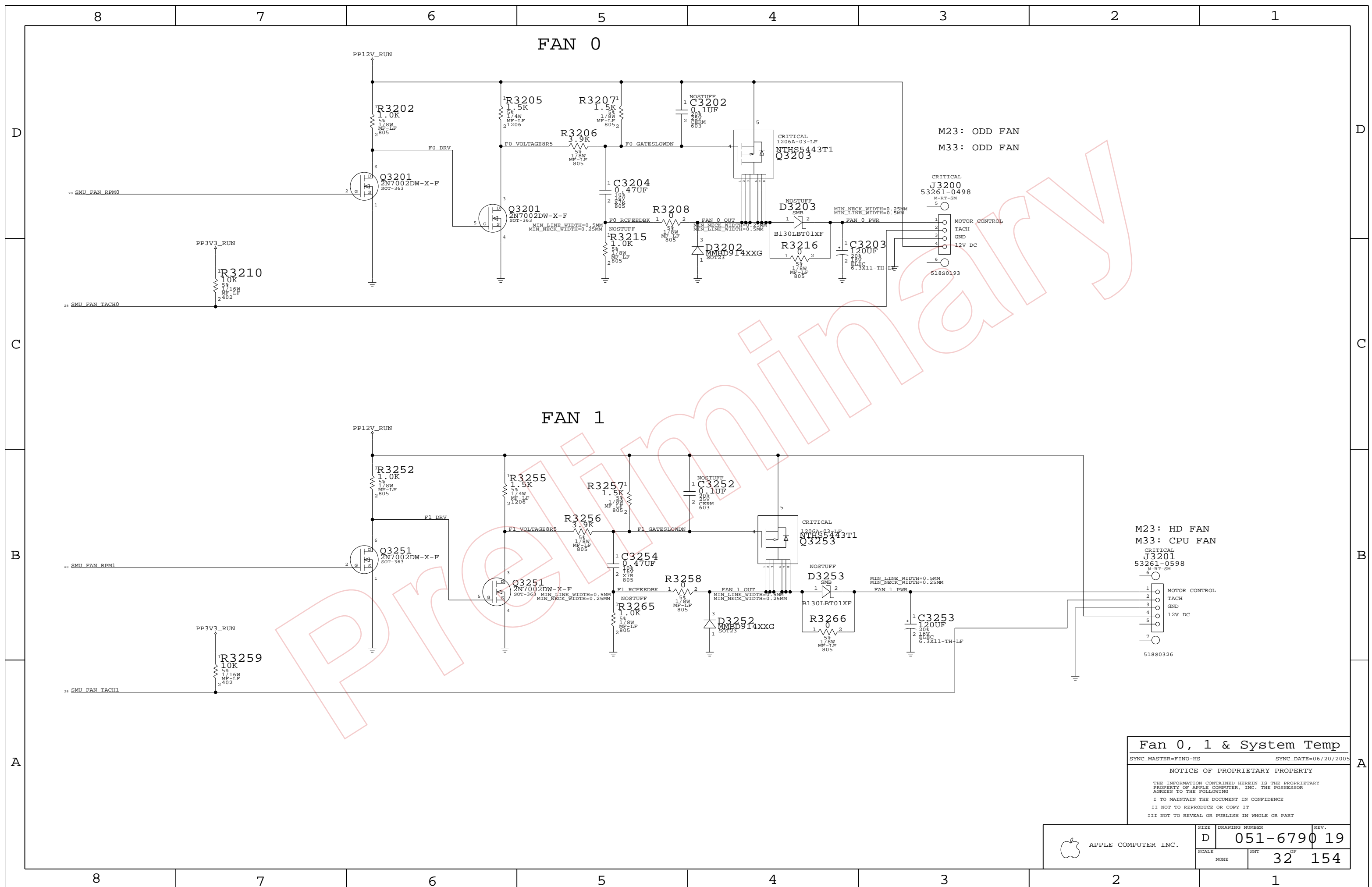
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-6790	REV. 19
SCALE NONE	SHT 31	OF 154



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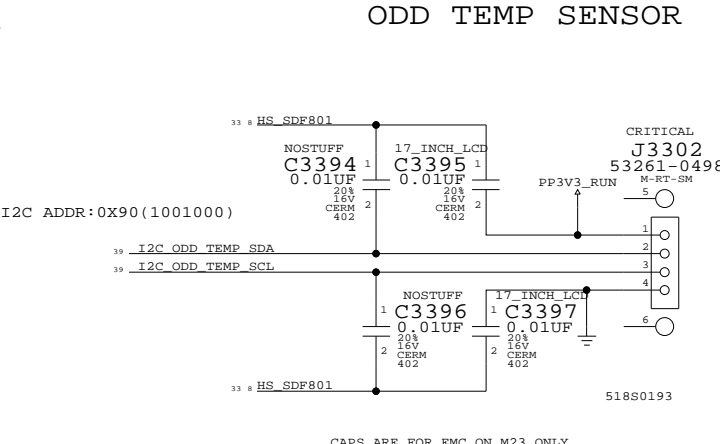
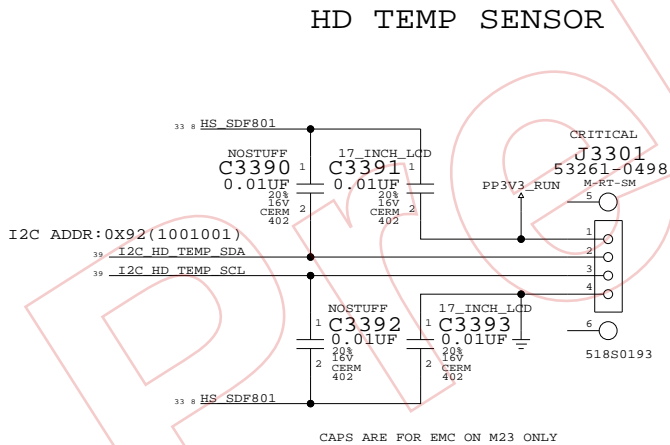
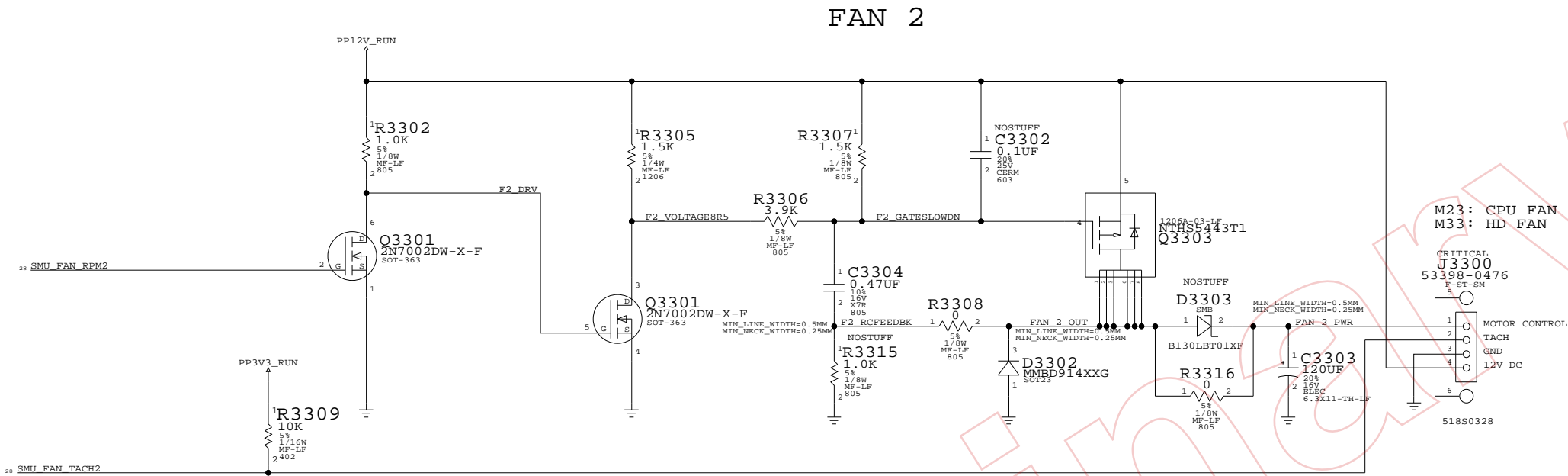
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A



Fan 2 & HD Temp

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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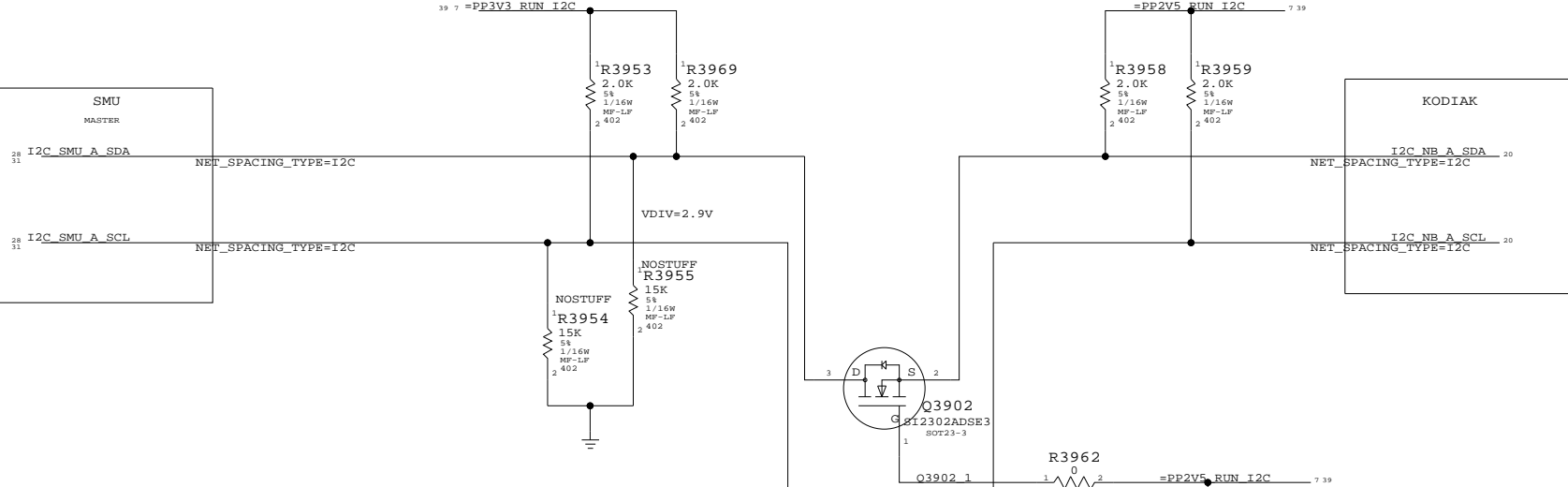
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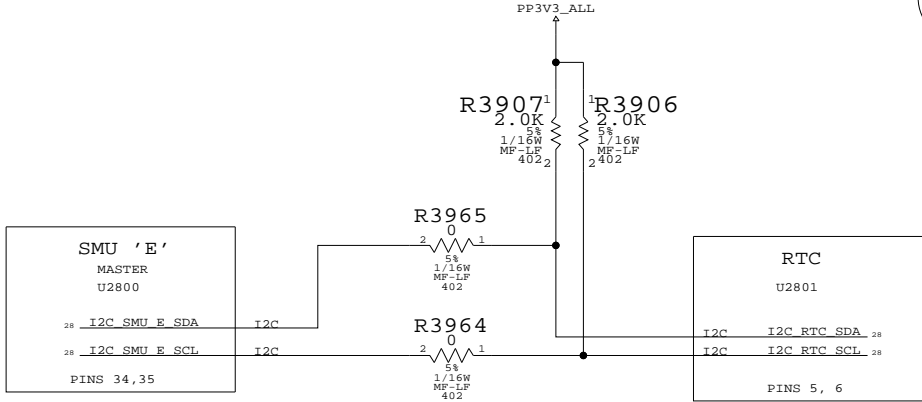
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	33 OF 154
NONE			

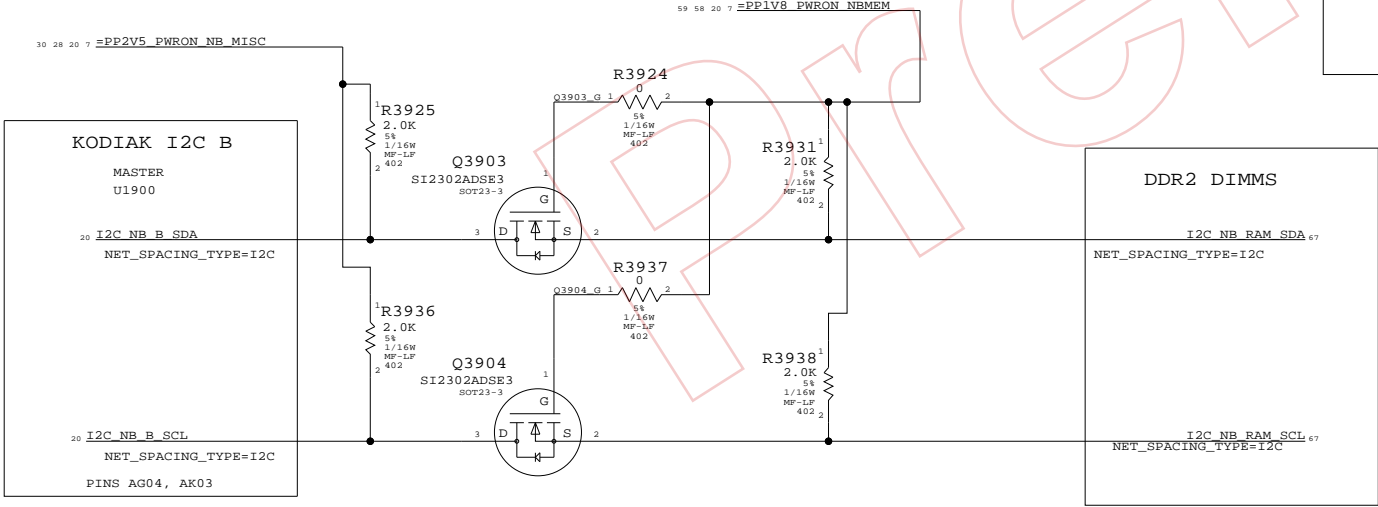
SMU AND NB I2C A BUS



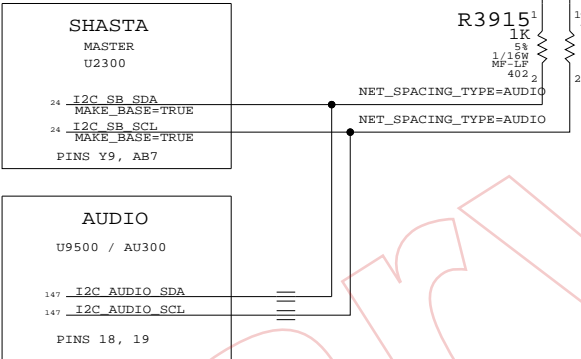
SMU I2C E BUS



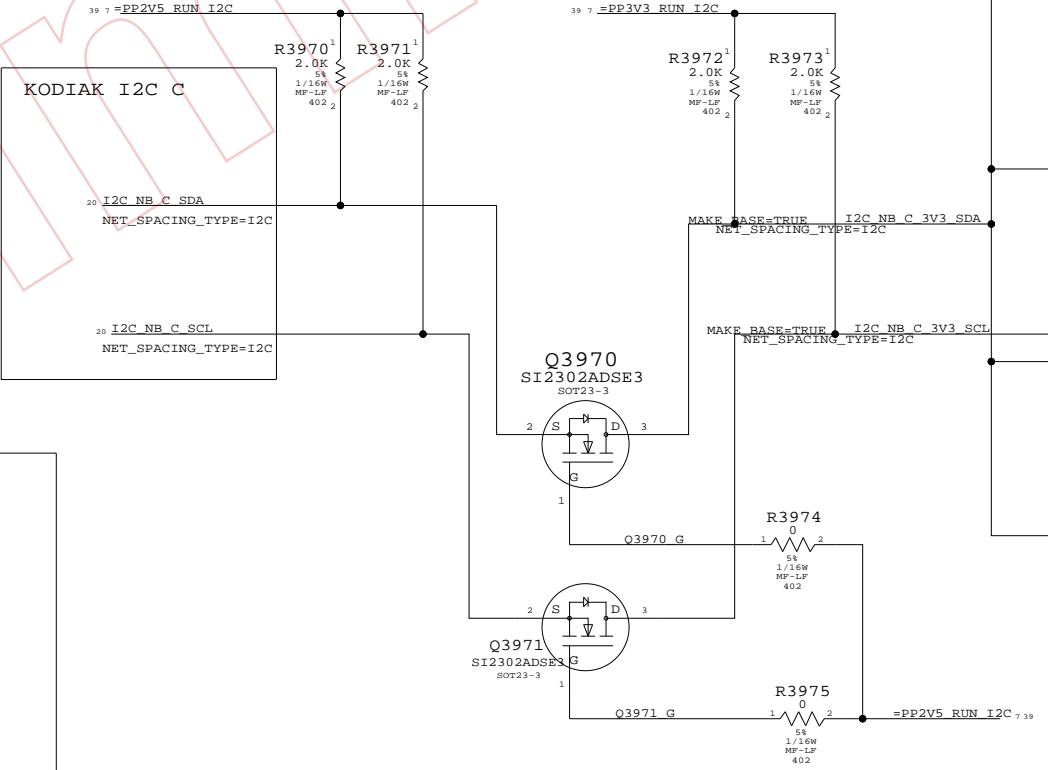
NB I2C B BUS



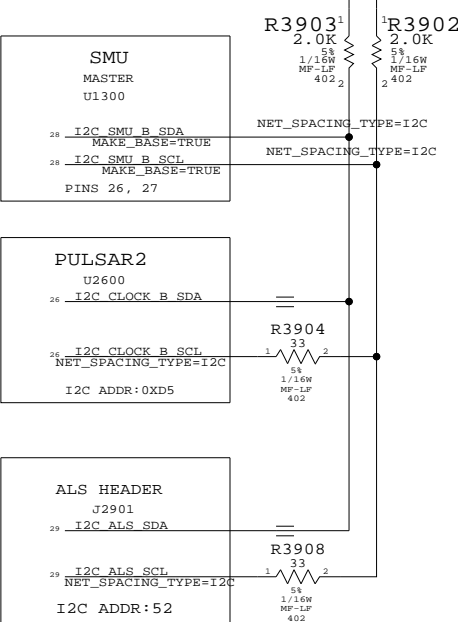
SB I2C BUS



NB I2C C BUS



SMU I2C B BUS



I2C Connections

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

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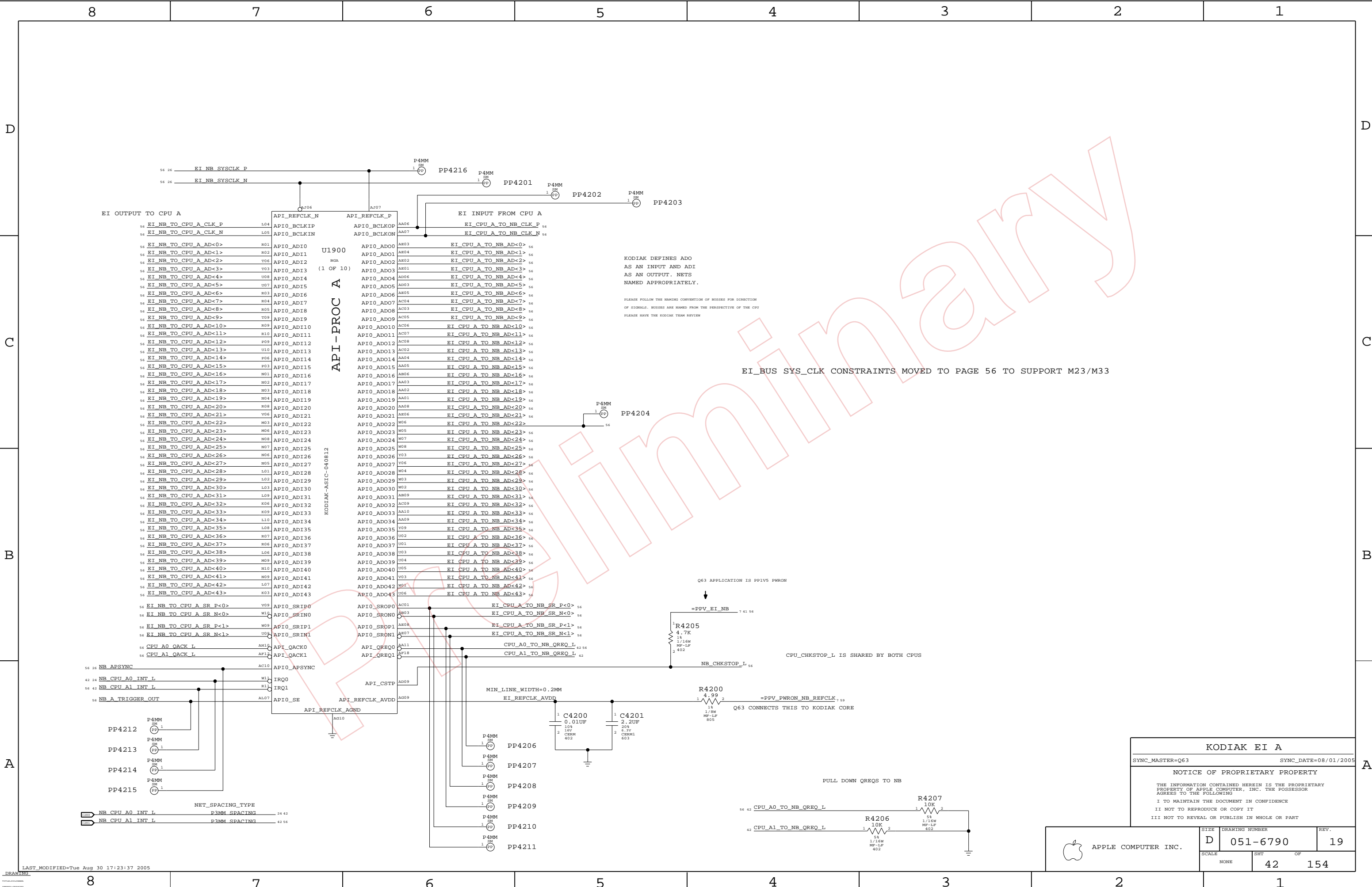
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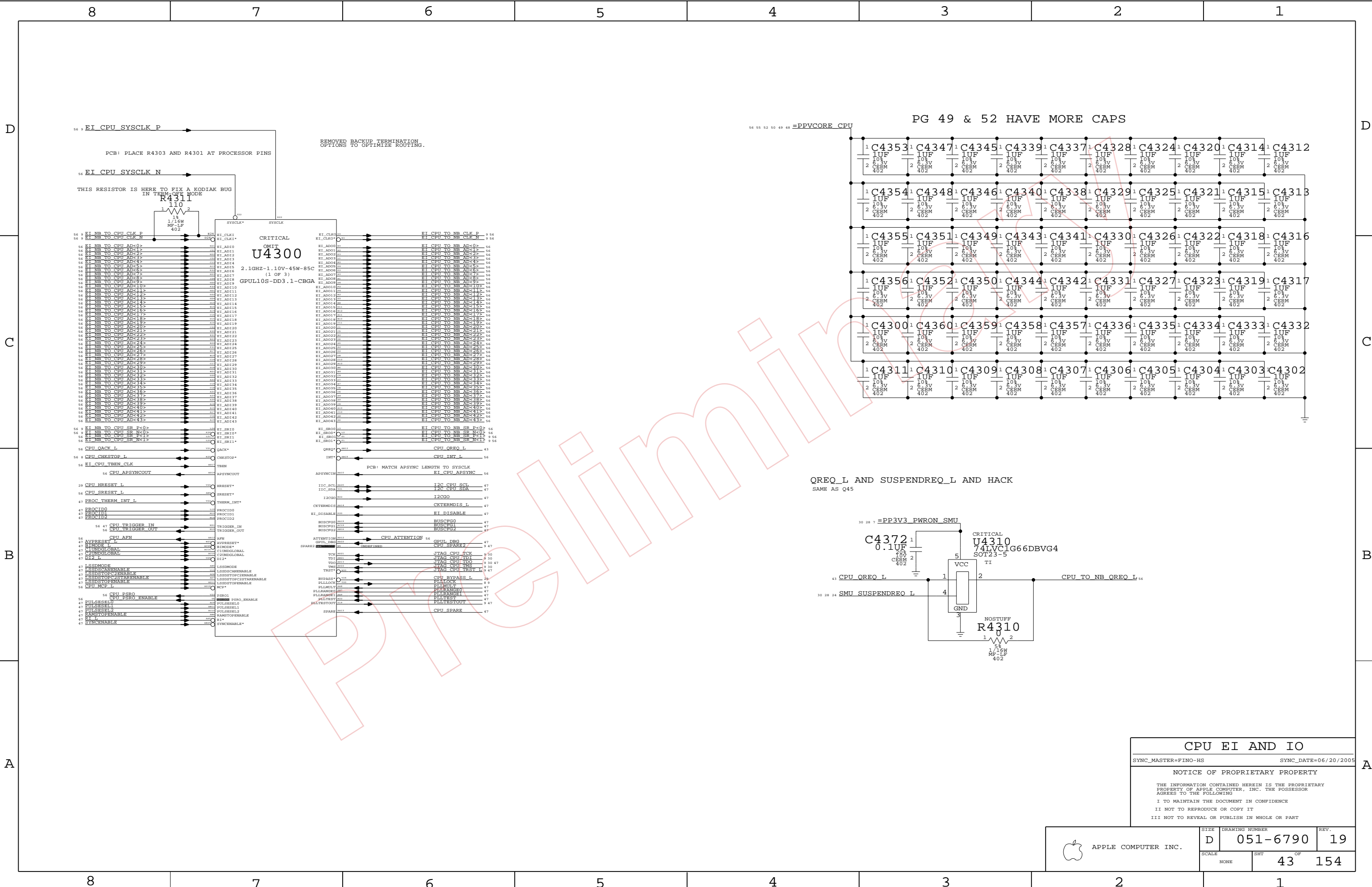
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SYNC_MASTER=Q63		SYNC_DATE=08/01/2005
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NONE		42	154



CPU EI AND IO

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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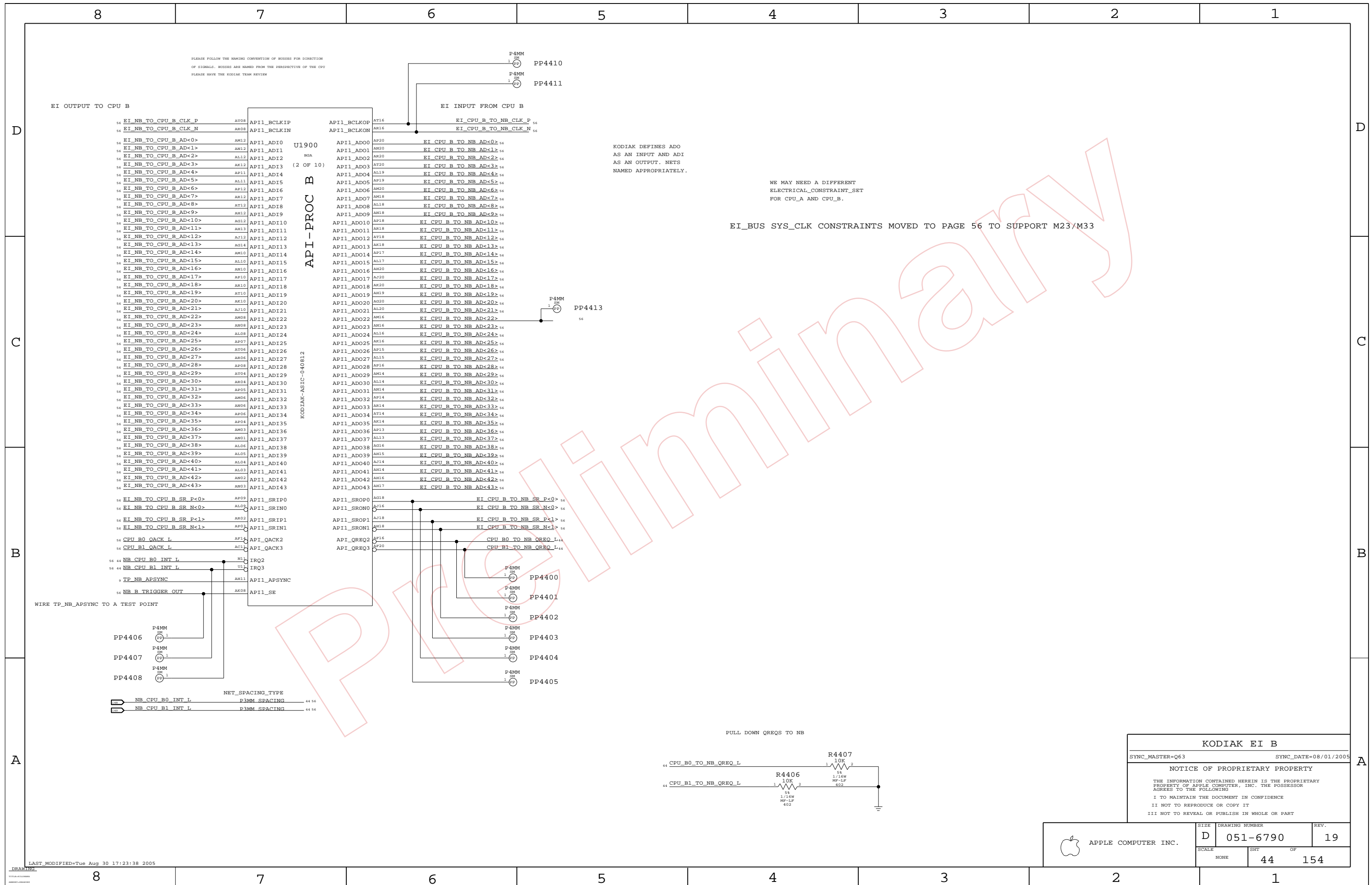
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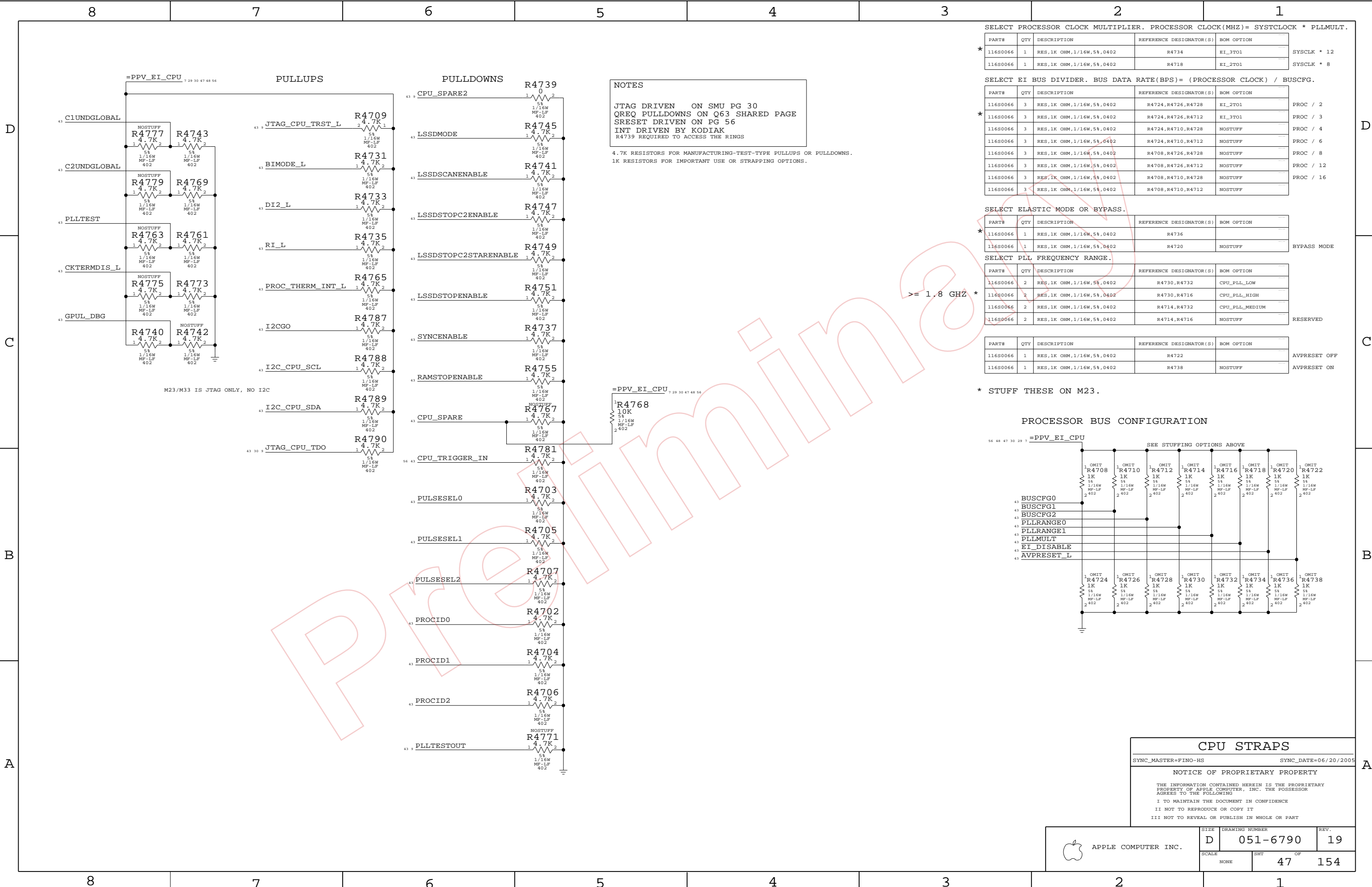
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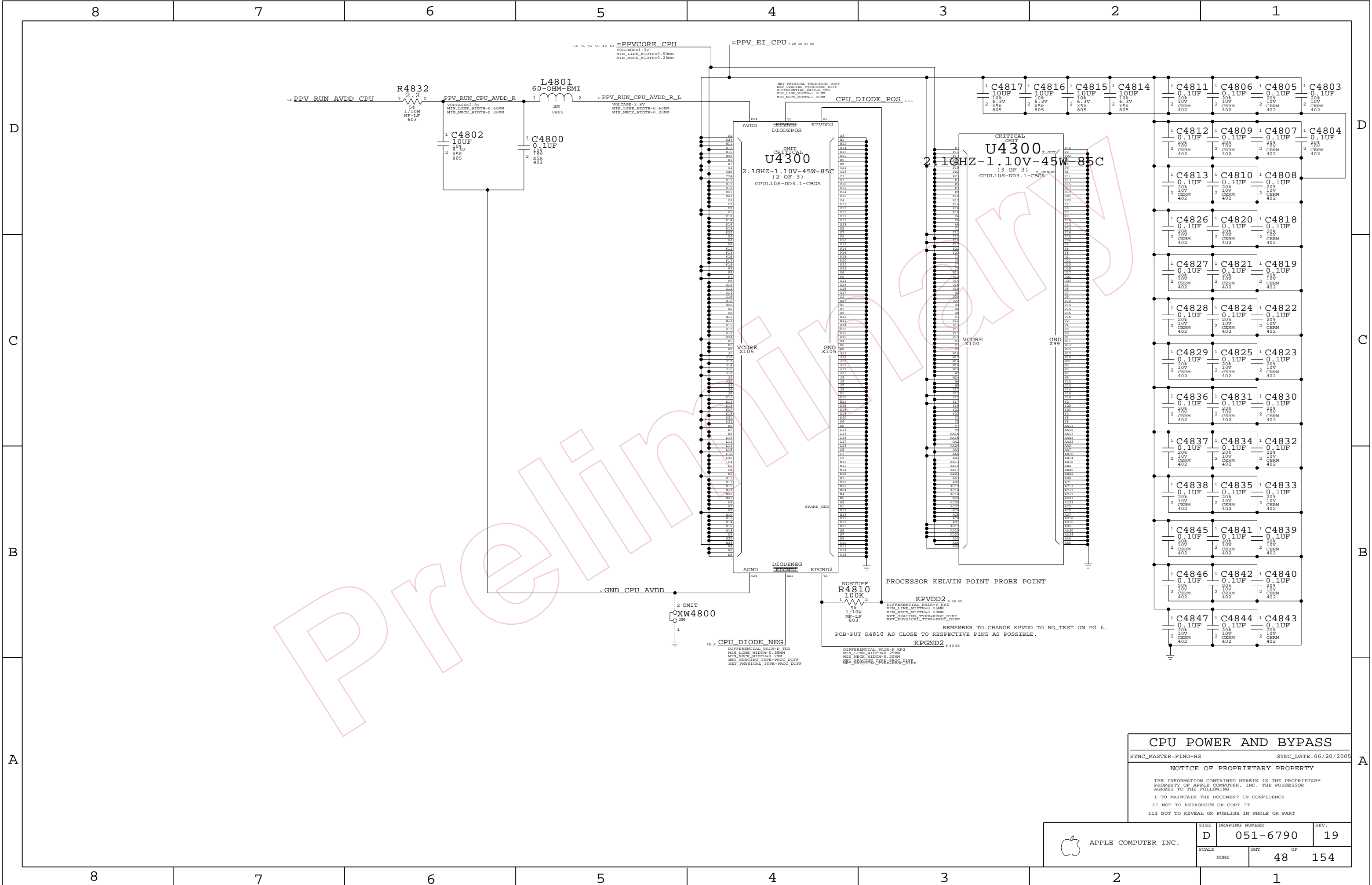
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SCALE	NONE		SHT
	43		OF 154







CPU POWER AND BYPASS

SYNC_MASTER=FINO-HS

SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

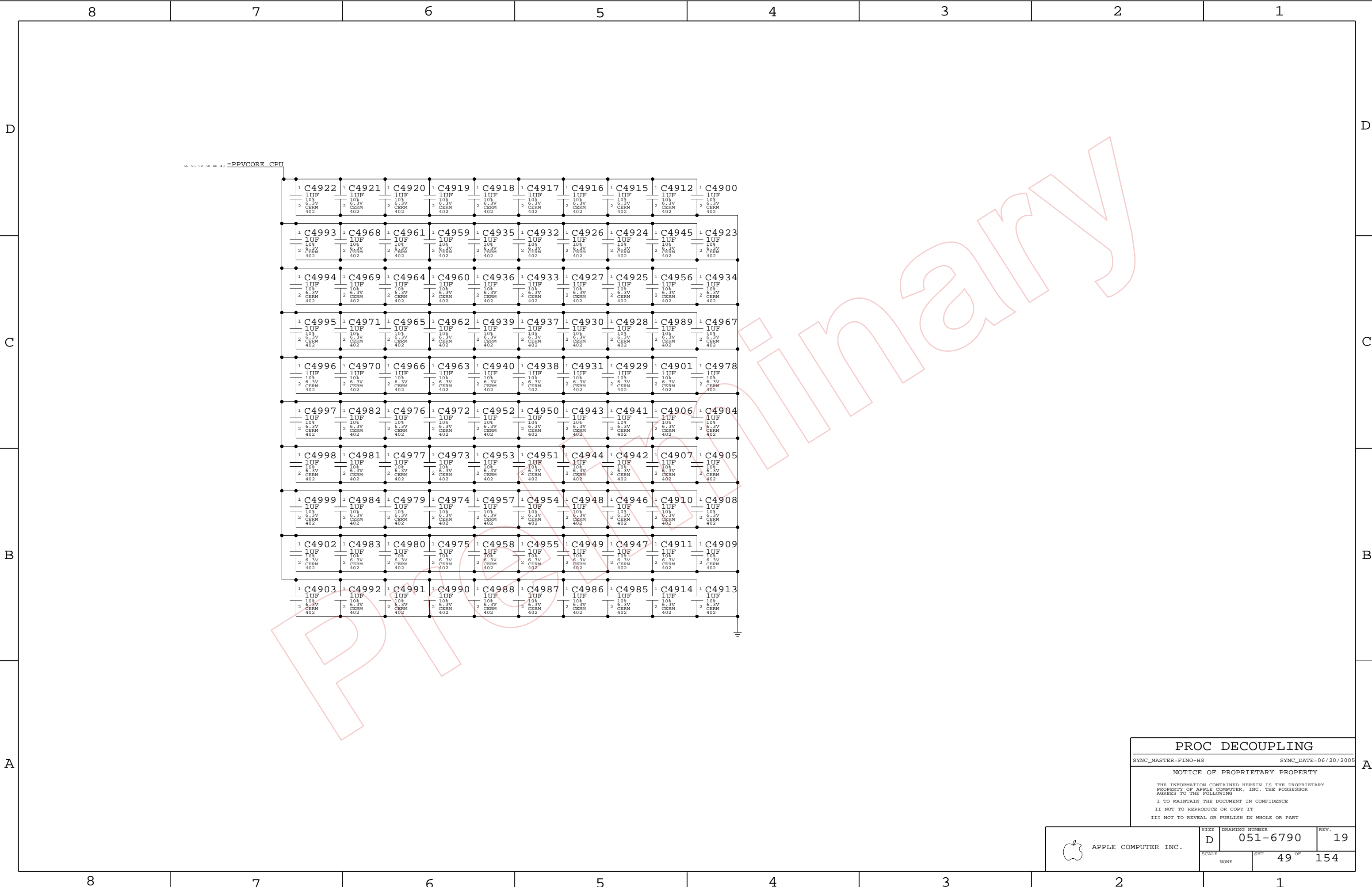
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NONE		48	154	



PROC DECOUPLING

SYNC_MASTER=FINO-HS

SYNC_DATE=06/20/2005


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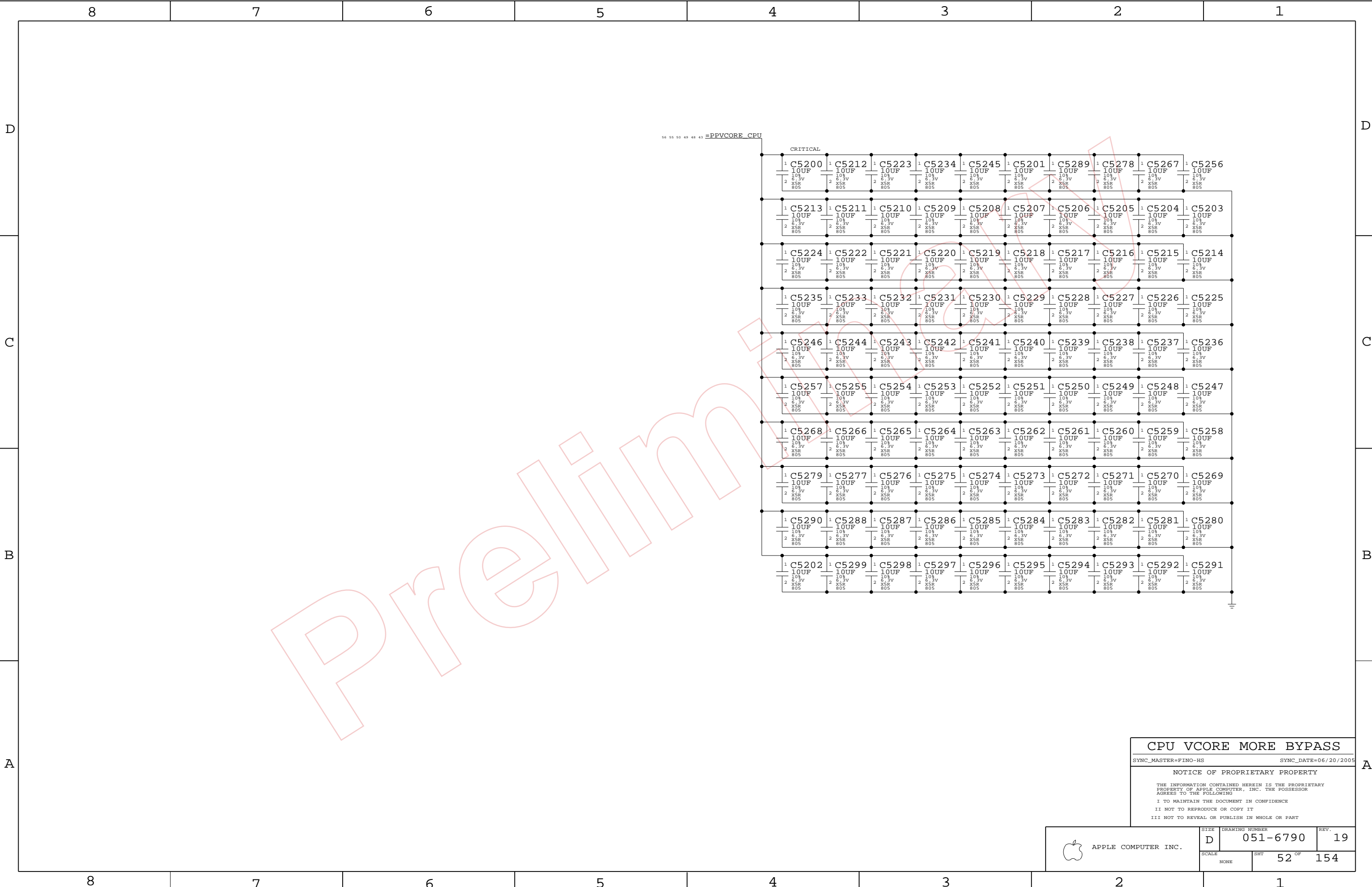
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NONE		49 OF	154



CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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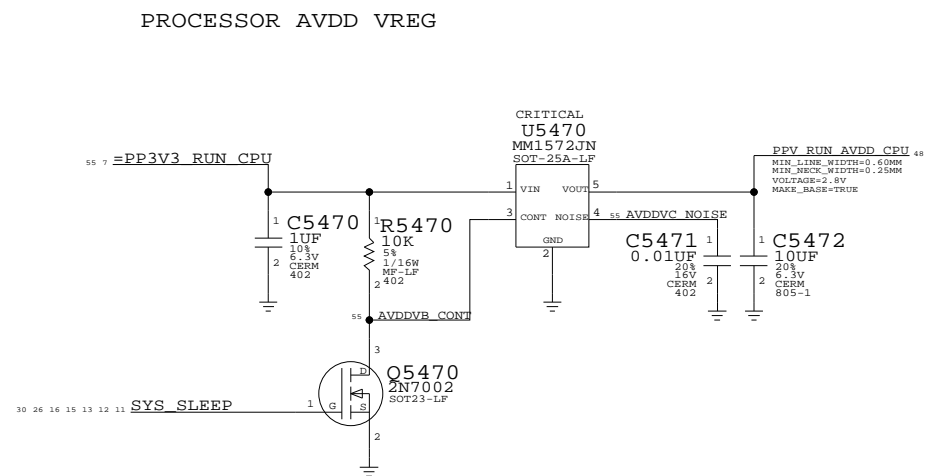
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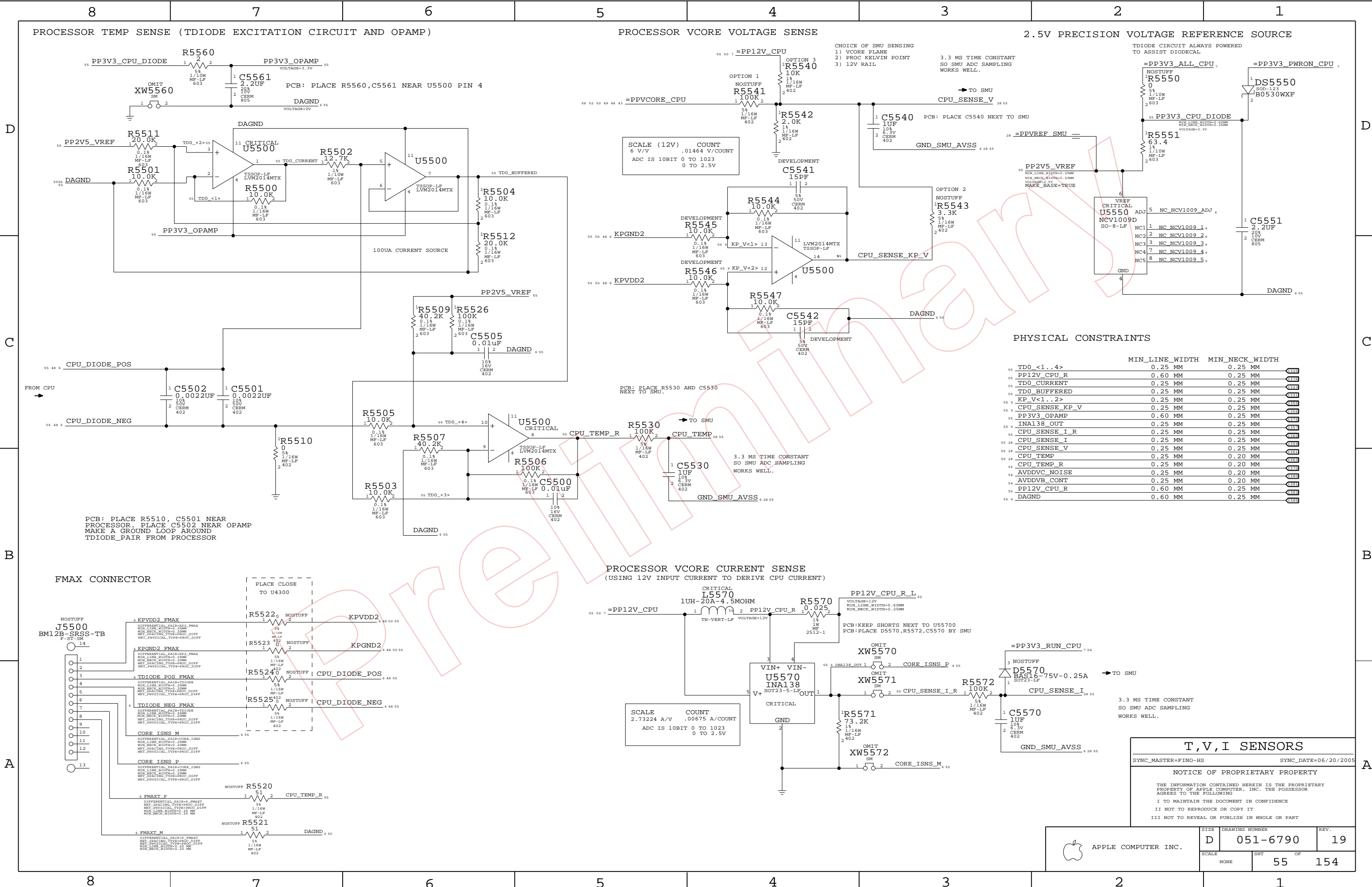
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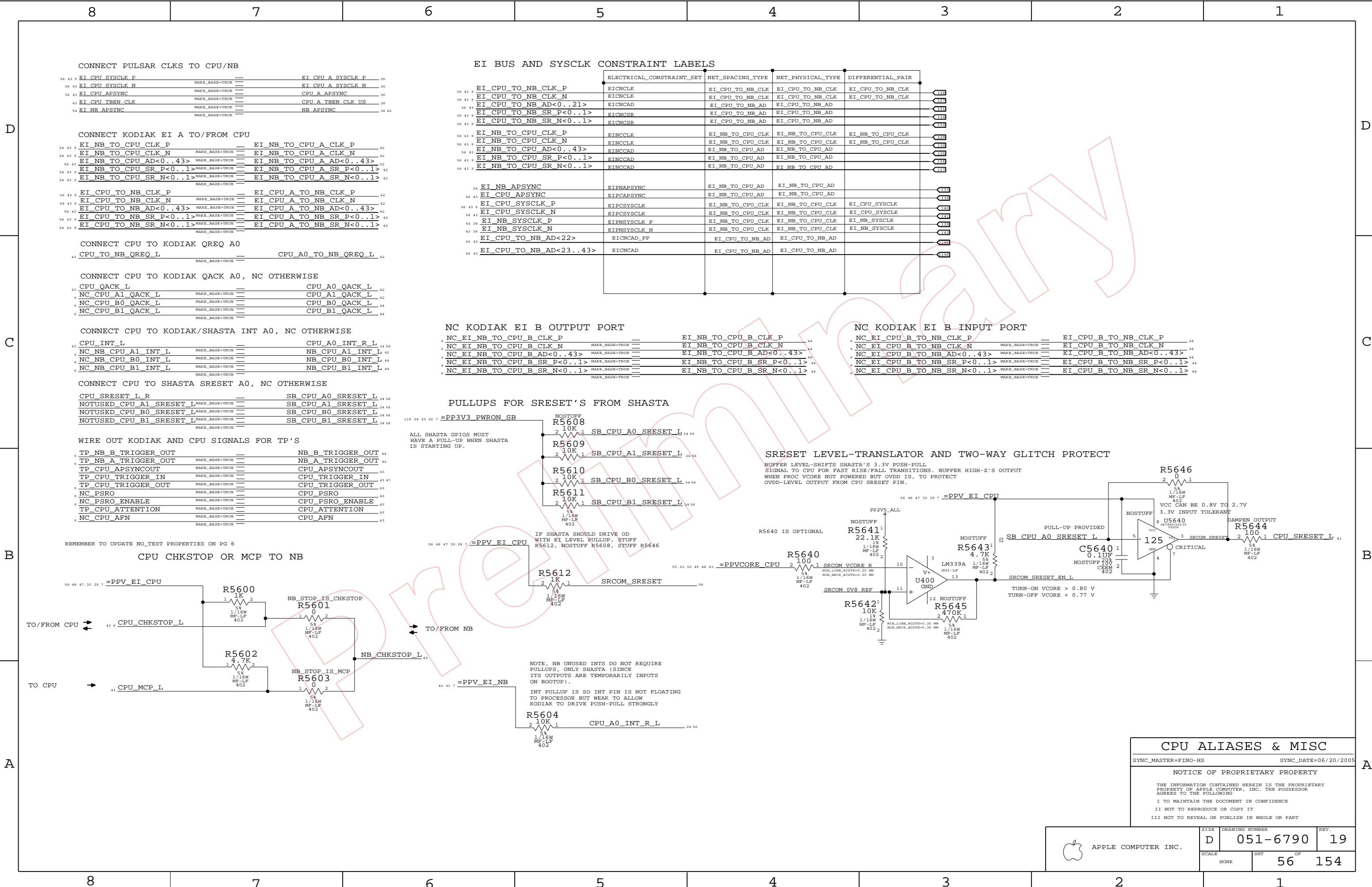
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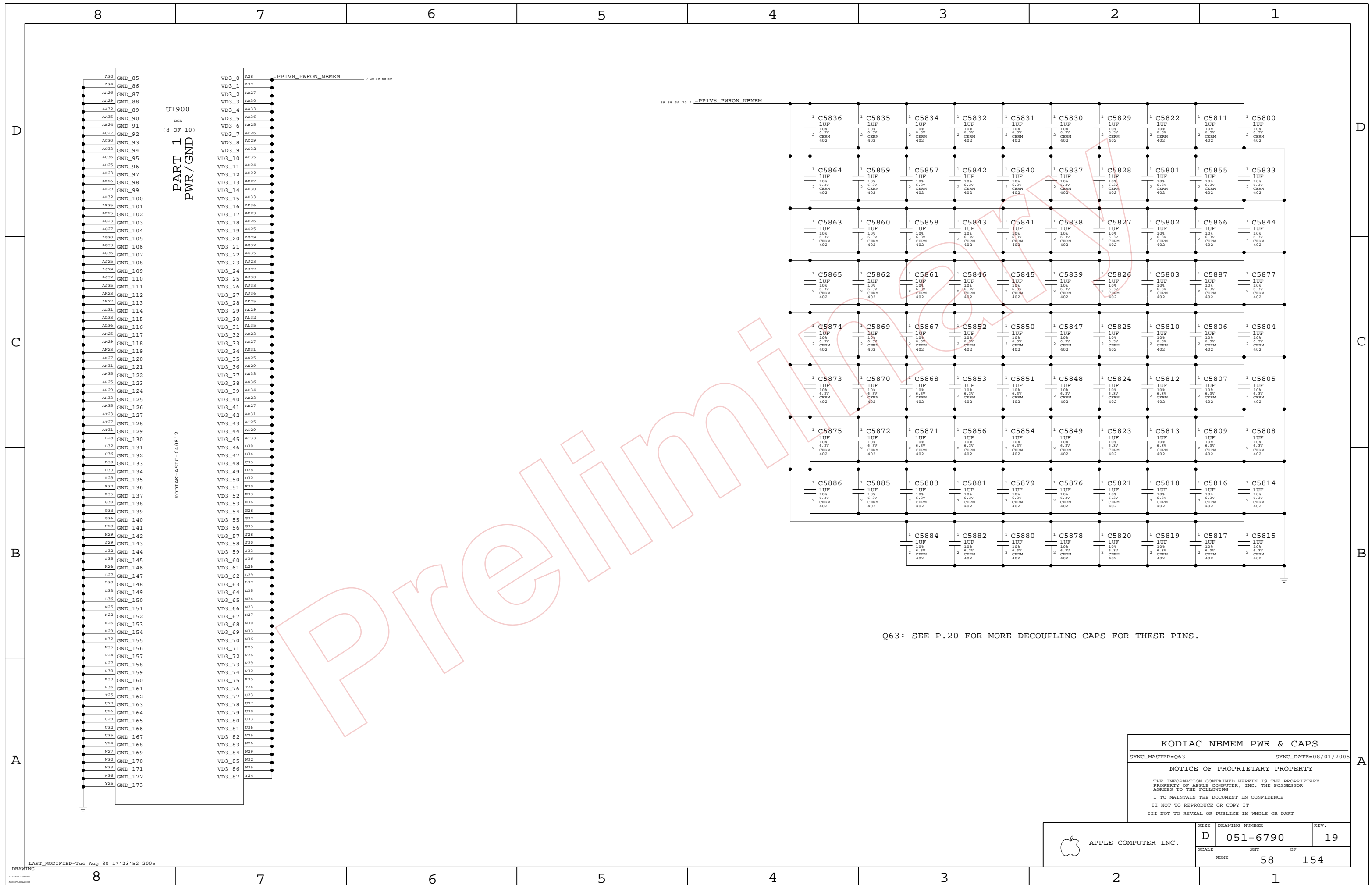
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	D	051-6790	19
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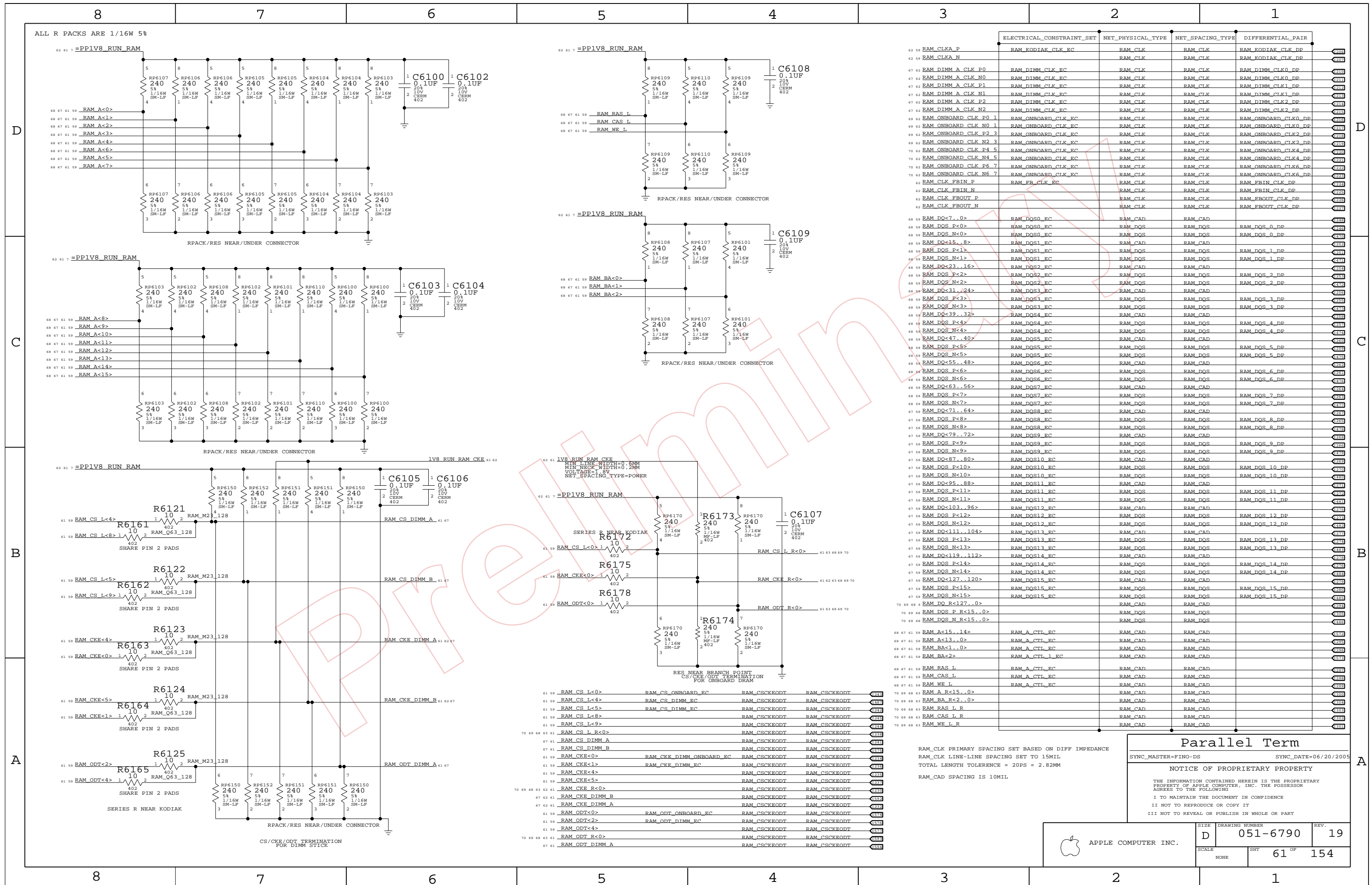


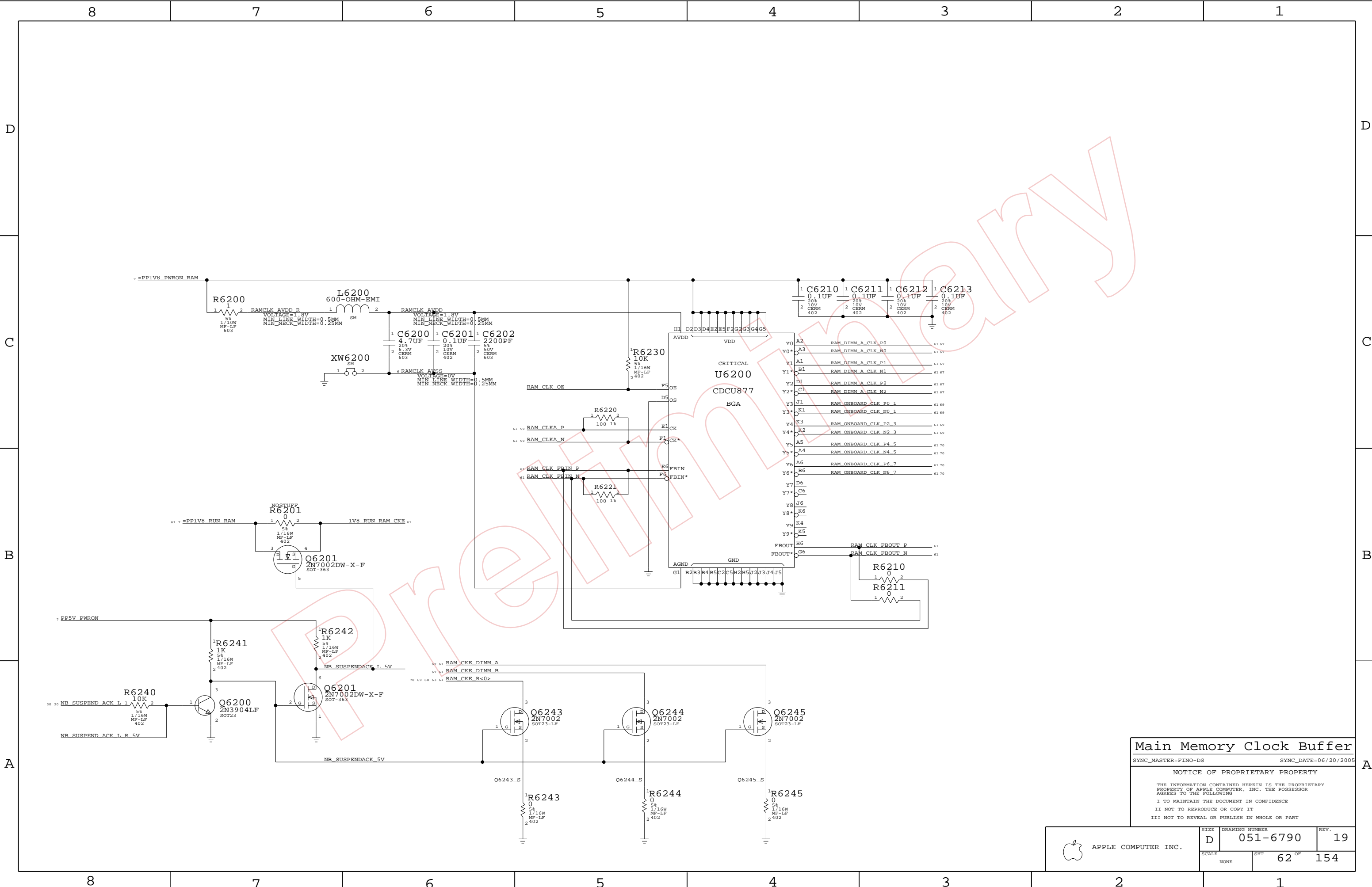
CPU AVDD VREG	
SYNC_MASTER=FINO-HS	SYNC_DATE=06/20/2005
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Main Memory Clock Buffer

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

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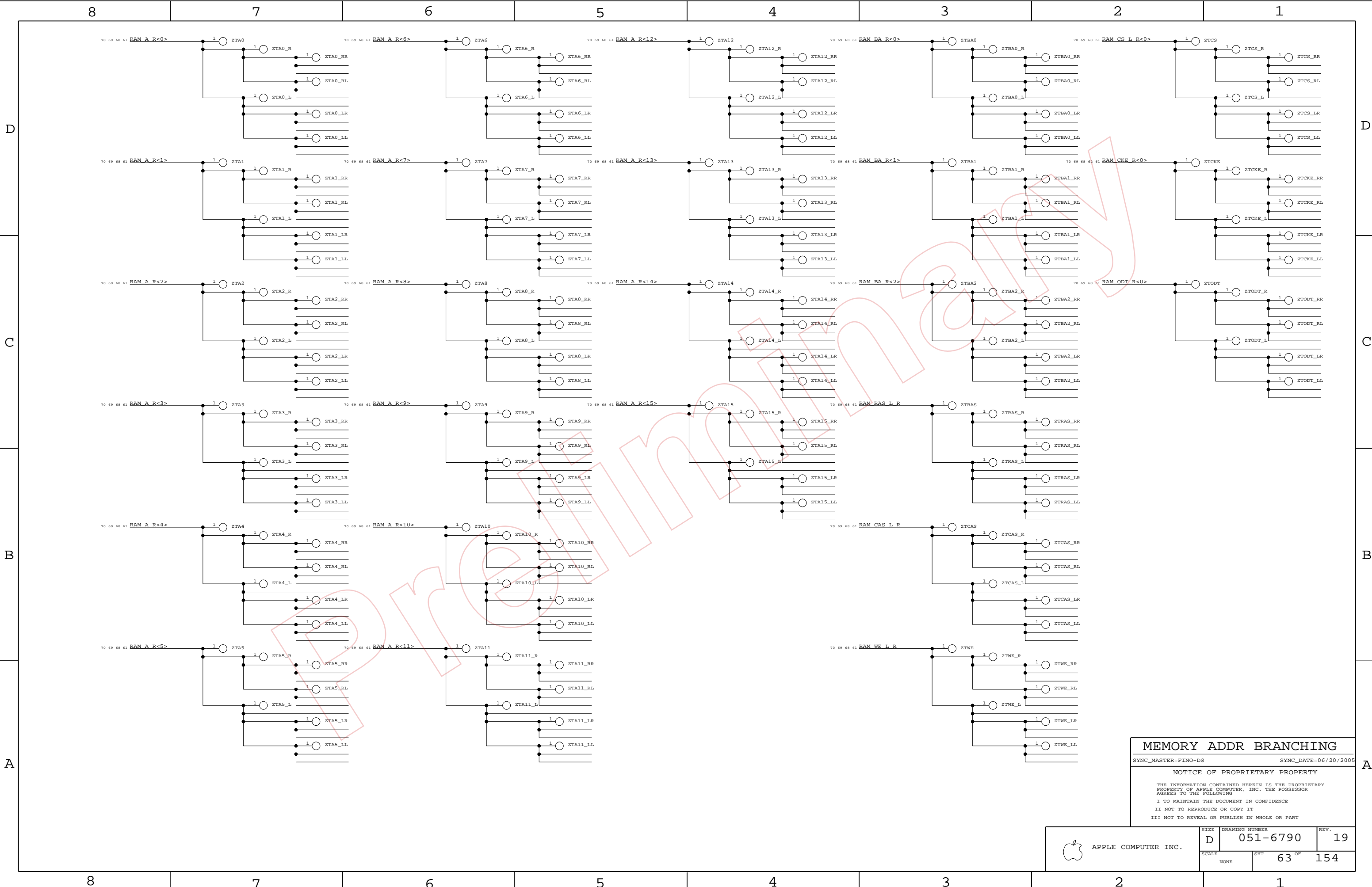
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	19
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NONE		



MEMORY ADDR BRANCHING

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

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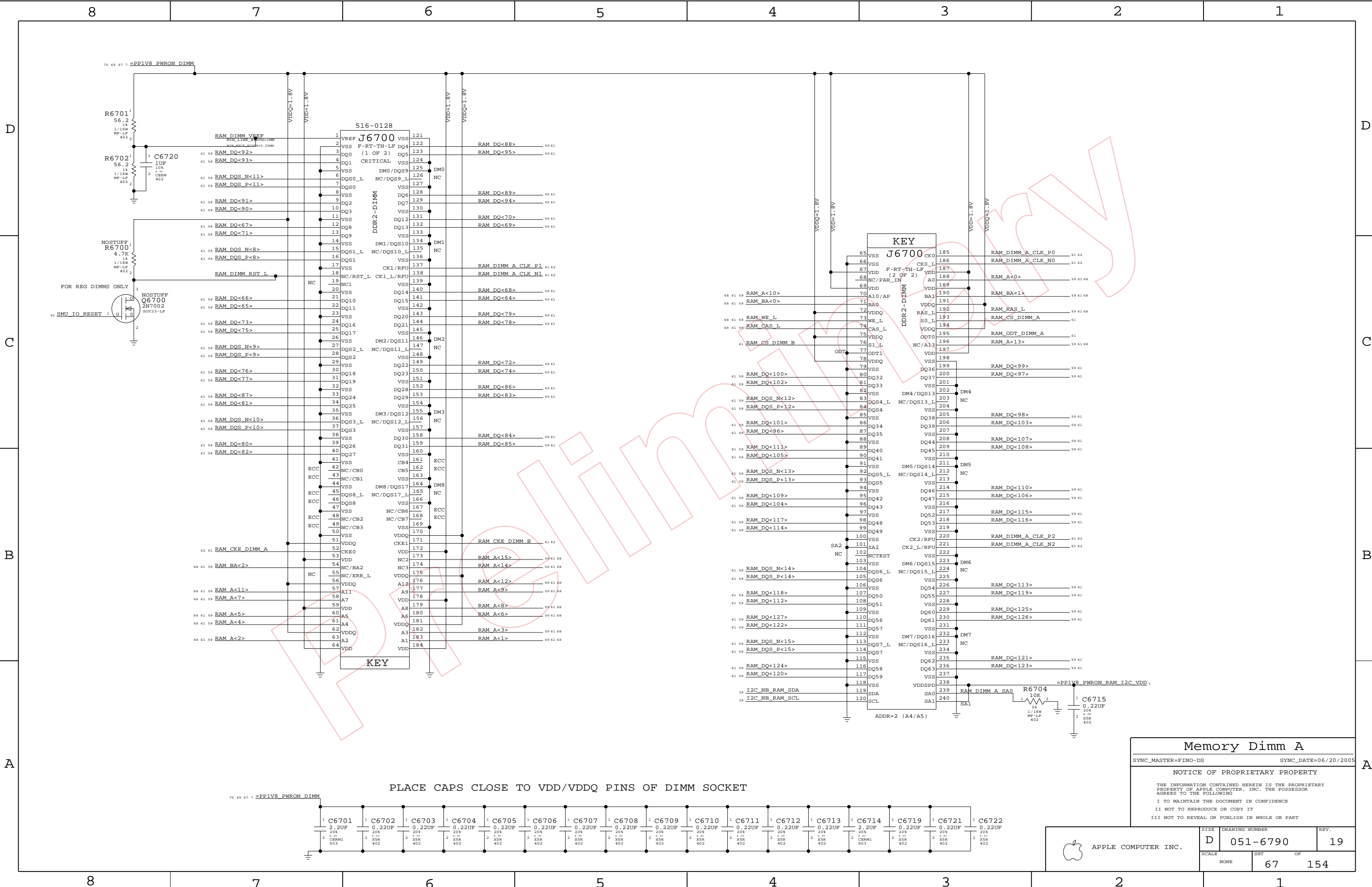
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SCALE		SHT	63 OF 154
NONE			



Memory Dimm A

SYNC_MASTER=FINO-DS

SYNC_DATE=06/20/2005

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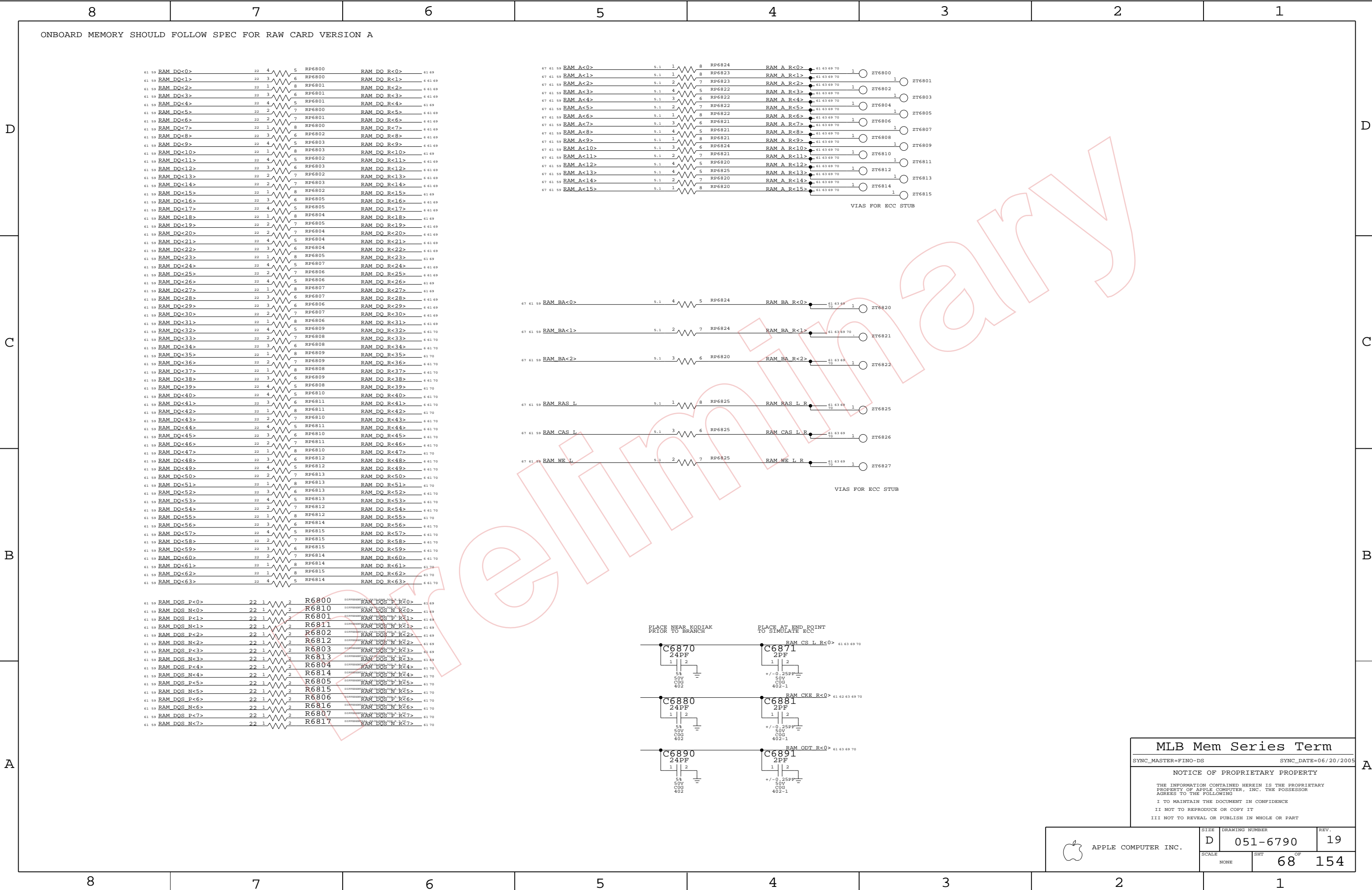
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SCALE		SHT	OF
NONE		67	154



MLB Mem Series Term

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

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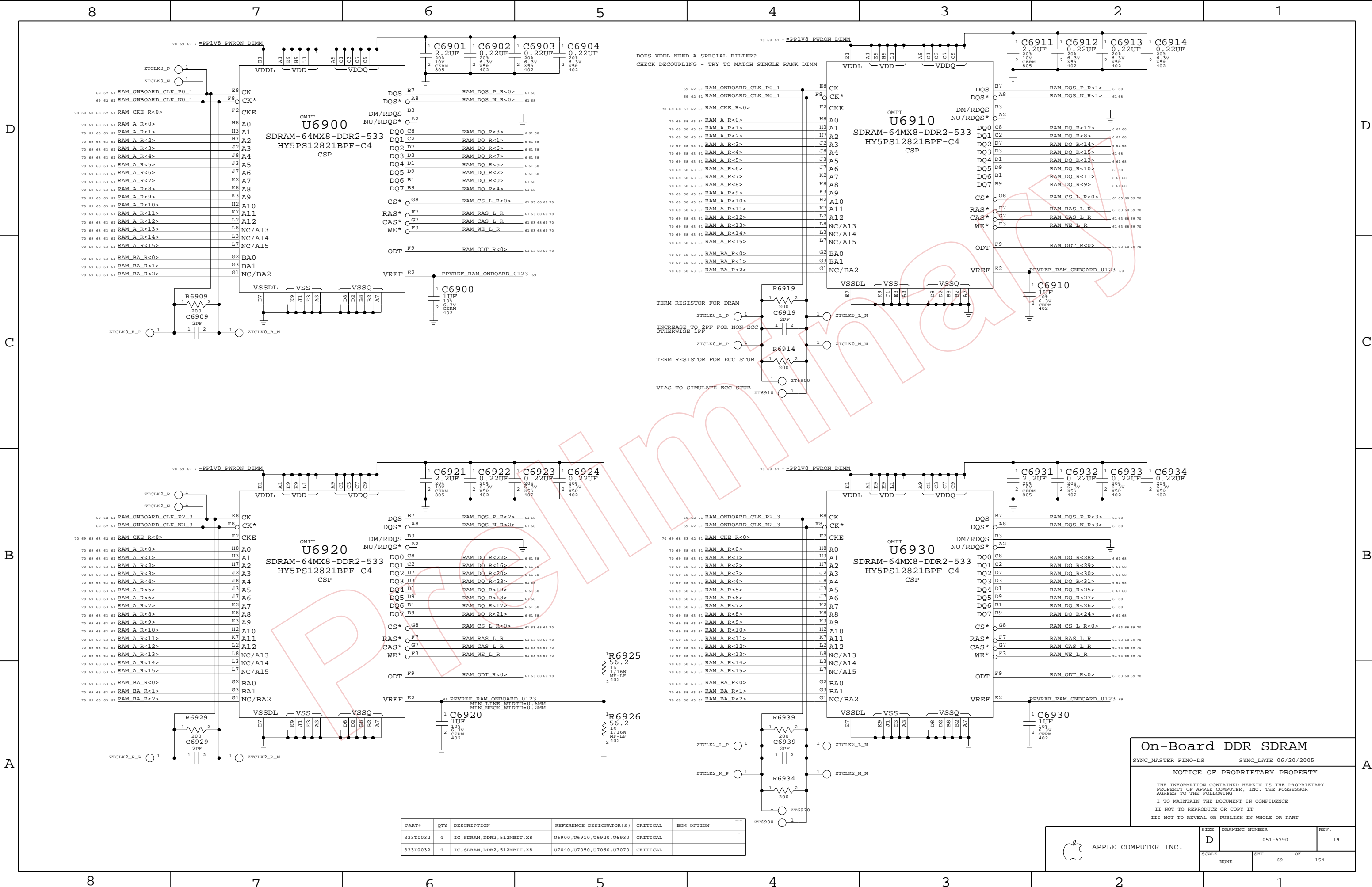
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	D	051-6790	19
SCALE	NONE	SHT	68 OF 154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333T0032	4	IC, SDRAM, DDR2, 512MBIT, X8	U6900, U6910, U6920, U6930	CRITICAL	
333T0032	4	IC, SDRAM, DDR2, 512MBIT, X8	U7040, U7050, U7060, U7070	CRITICAL	

On-Board DDR SDRAM

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

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051-6790

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SCALE

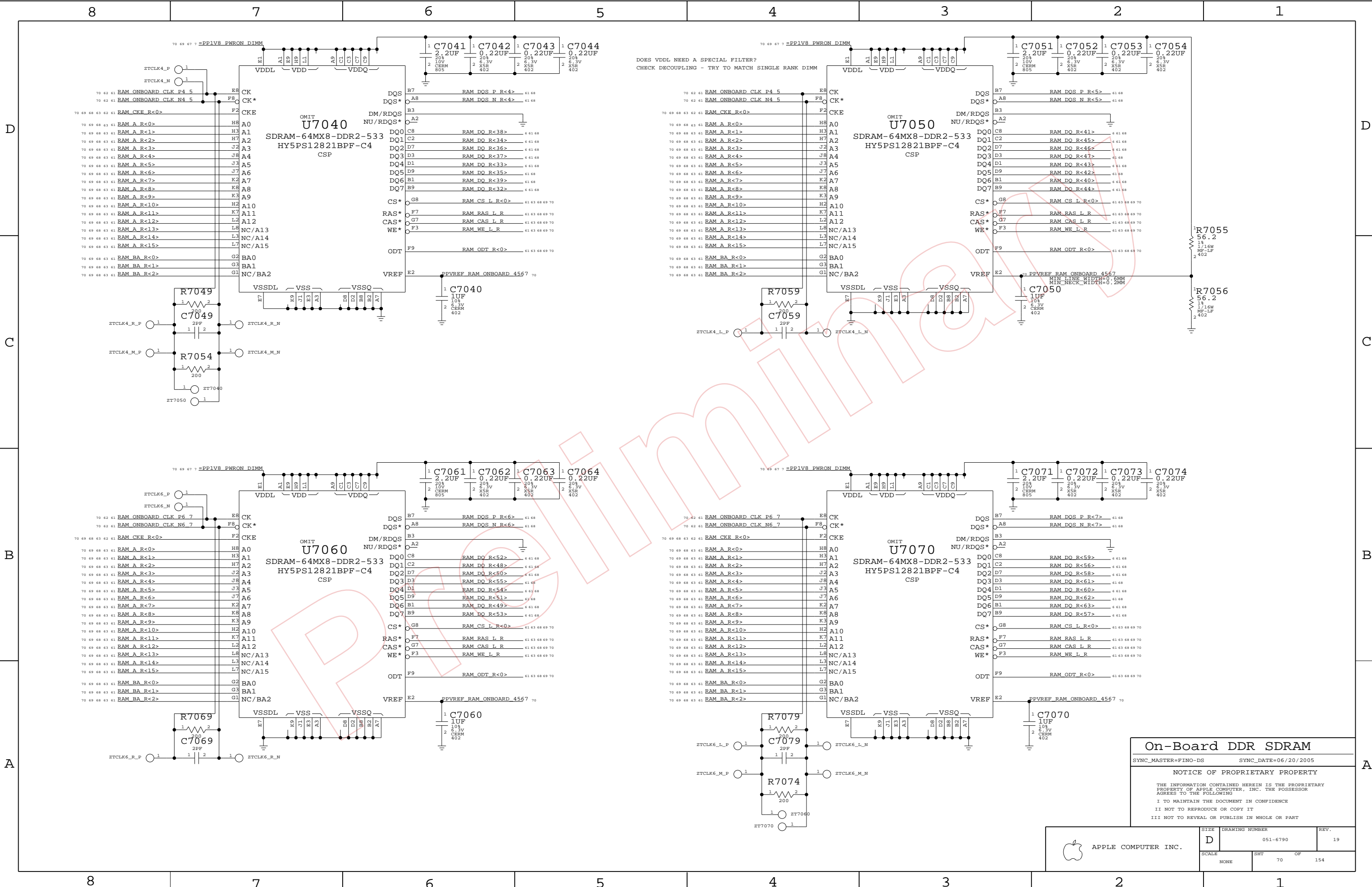
NONE

SHT

69

OF

154



On-Board DDR SDRAM

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

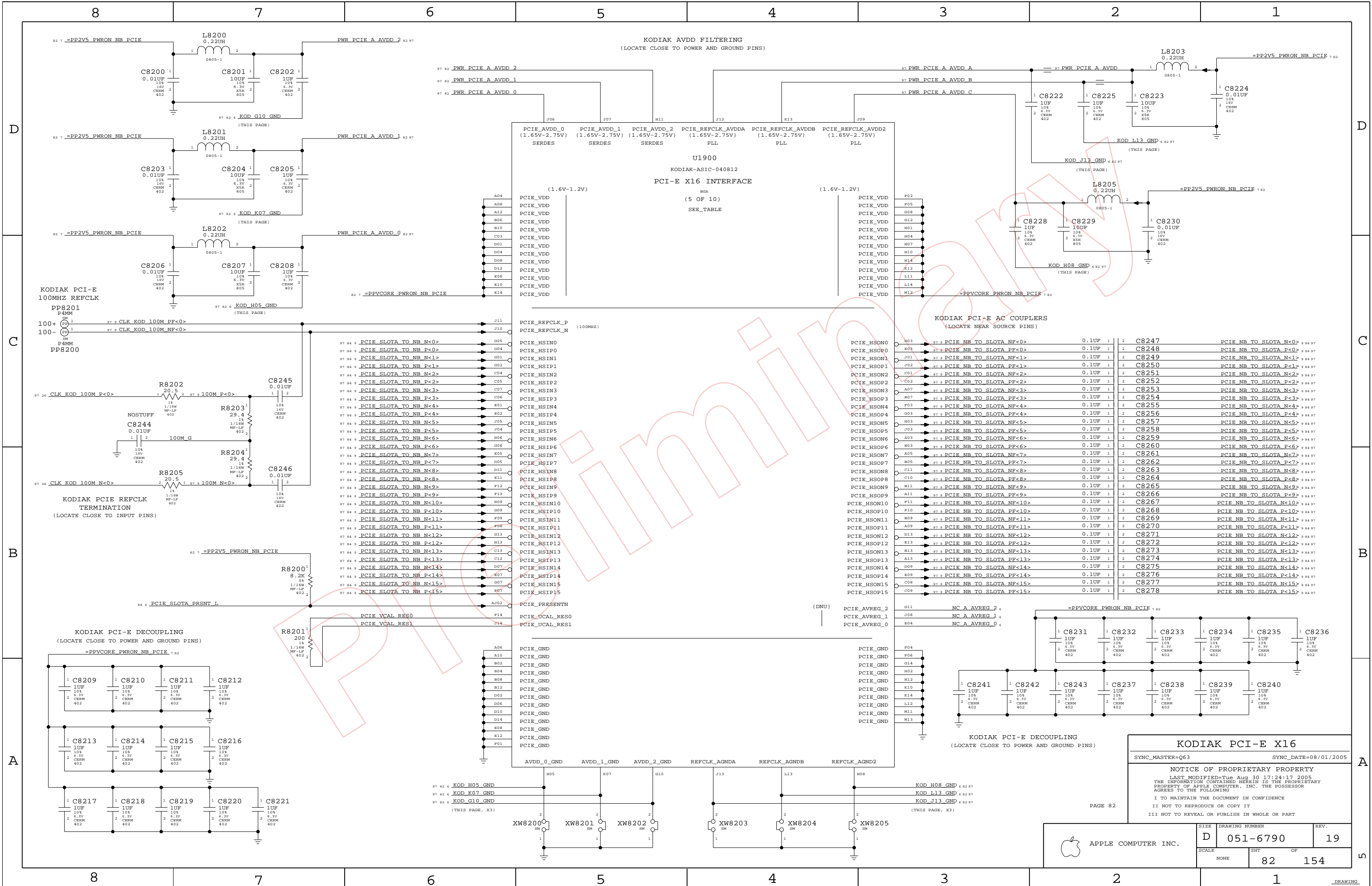
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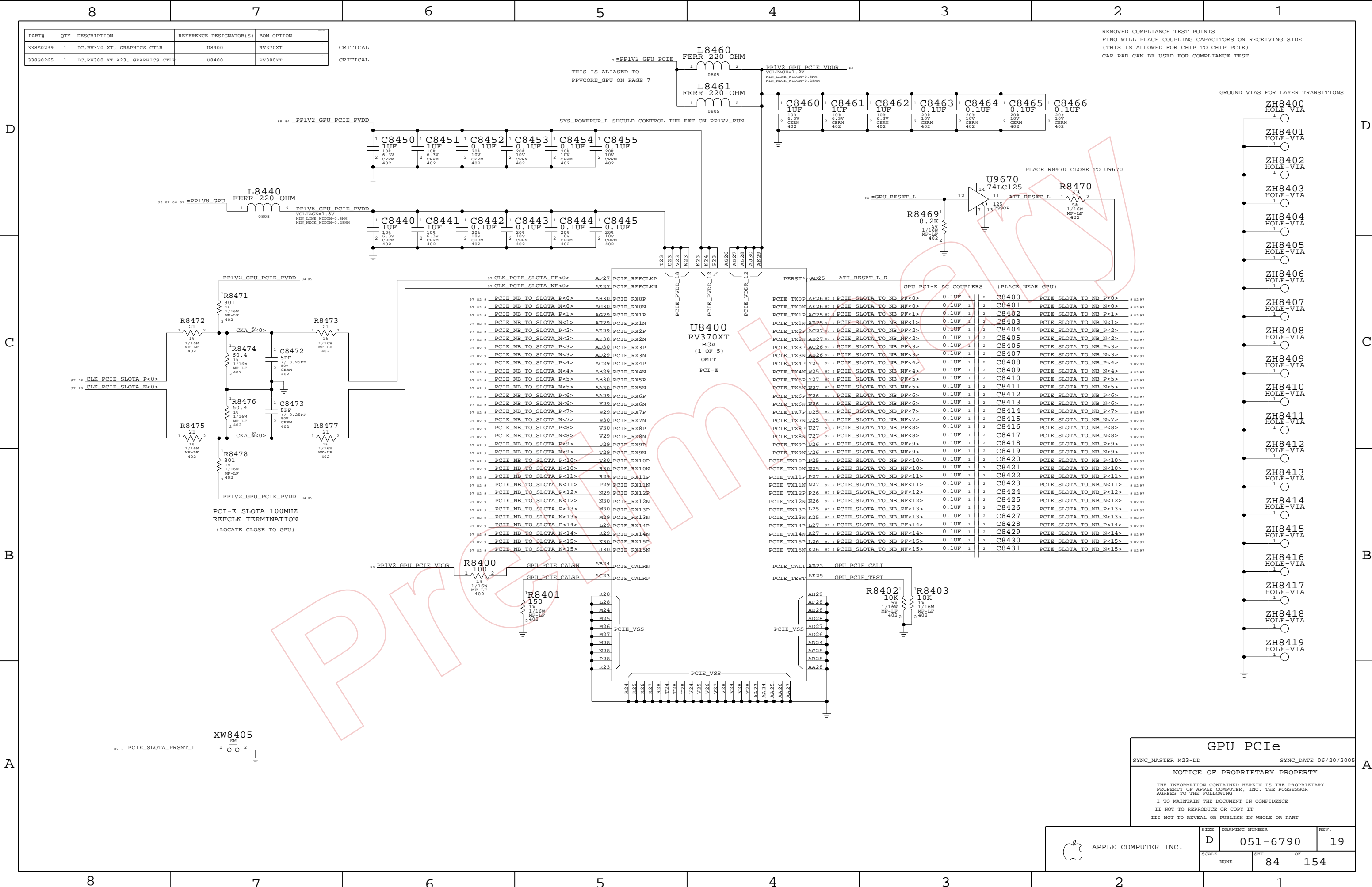
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. 19
	SCALE NONE	SHT 70	OF 154





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0239	1	IC,RV370 XT, GRAPHICS CTRL	U8400	RV370XT
338S0265	1	IC,RV380 XT A23, GRAPHICS CTRL	U8400	RV380XT

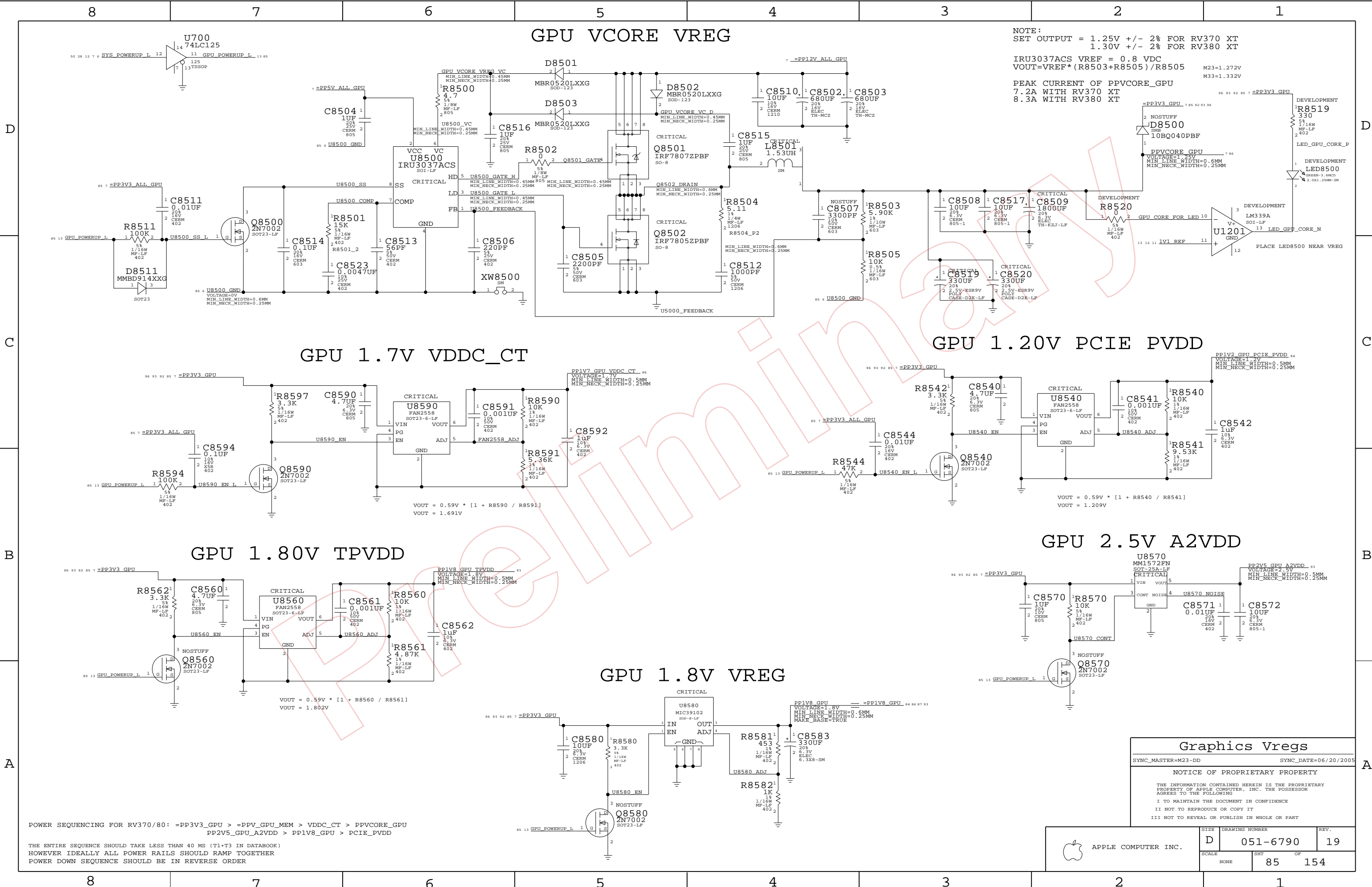
CRITICAL
CRITICAL

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIe)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

GROUND VIAS FOR LAYER TRANSITIONS

GPU PCIe	
SYNC_MASTER=M23-DD	SYNC_DATE=06/20/2005
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. 19
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GPU VCORE VREG

NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT
IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505
M23=1.272V
M33=1.332V
PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

GPU 1.7V VDDC_CT

GPU 1.20V PCIE PVDD

GPU 1.80V TPVDD

GPU 1.8V VREG

GPU 2.5V A2VDD

Graphics Vregs		
SYNC_MASTER=M23-DD		SYNC_DATE=06/20/2005
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POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD
THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	OF
NONE		85	154

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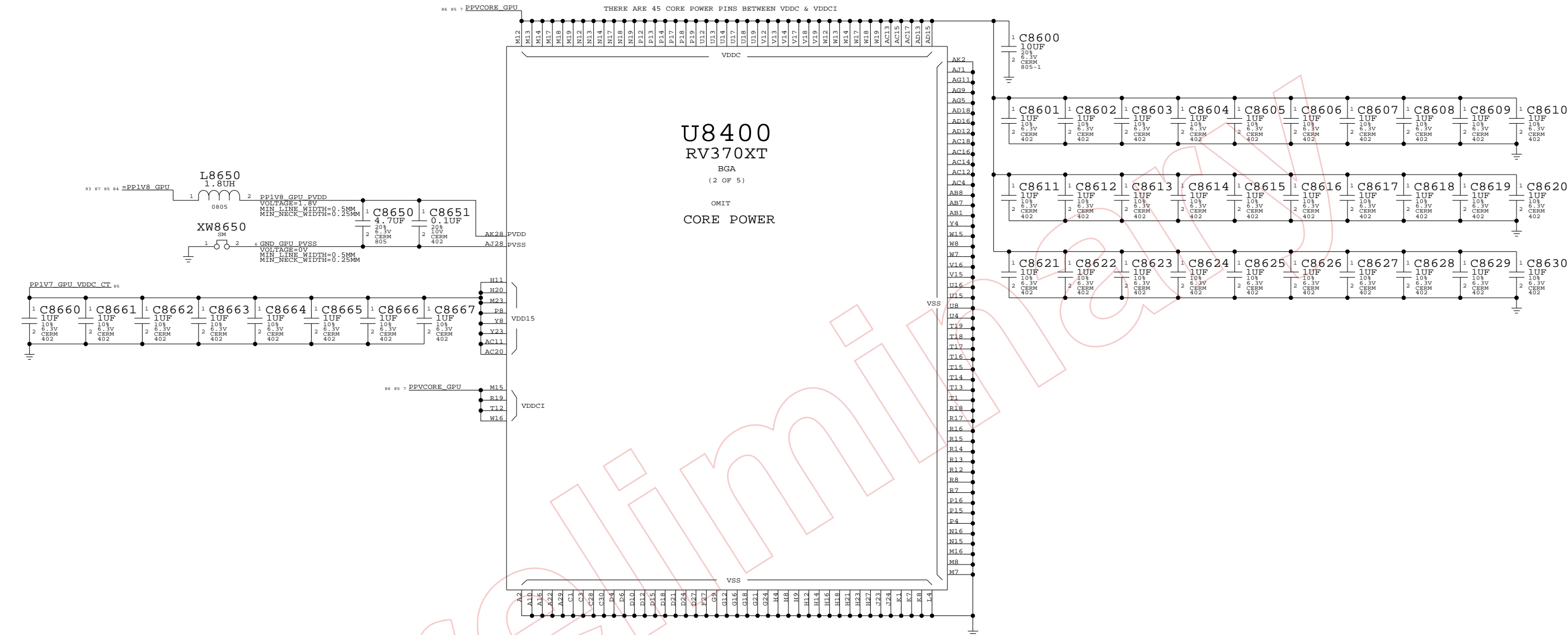
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GPU Core Power

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SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER		REV.
	D	051-6790		19
SCALE		SHT	OF	
NONE		86	154	

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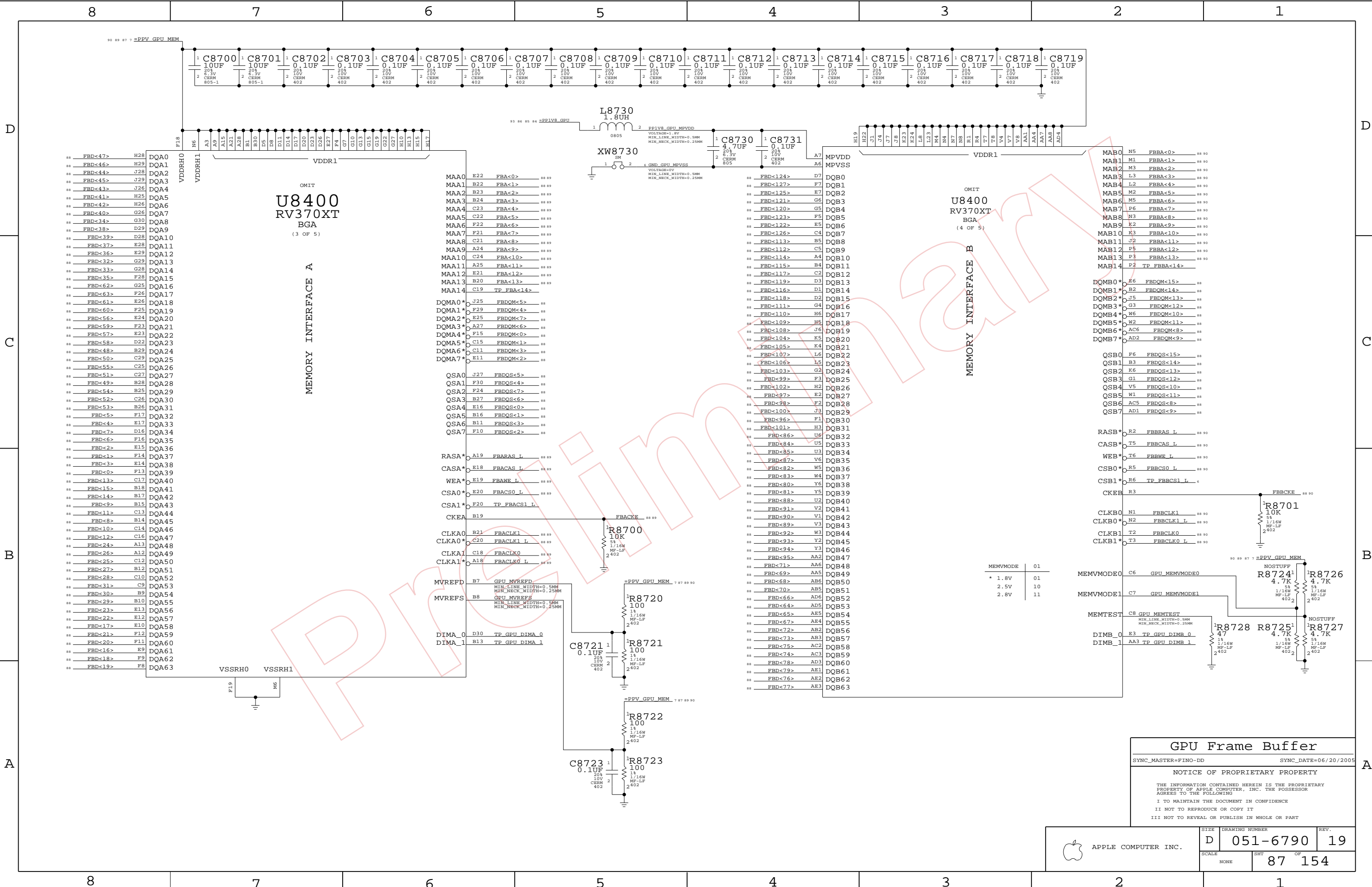
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MEMVMODE	01
* 1.8V	01
2.5V	10
2.8V	11

GPU Frame Buffer

SYNC_MASTER=FINO-DD

SYNC_DATE=06/20/2005

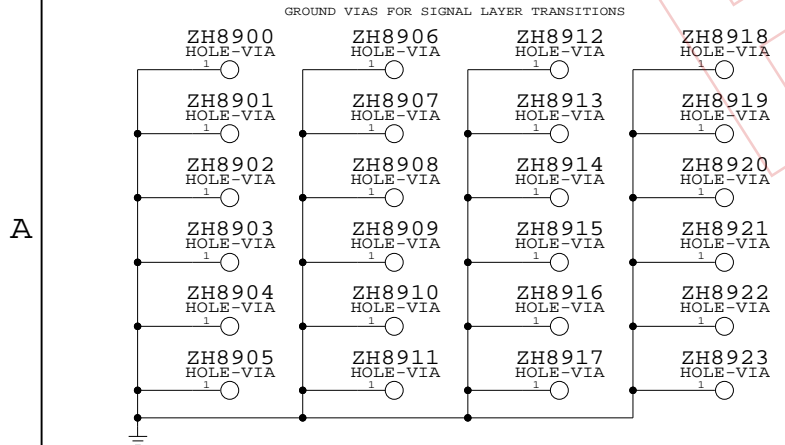
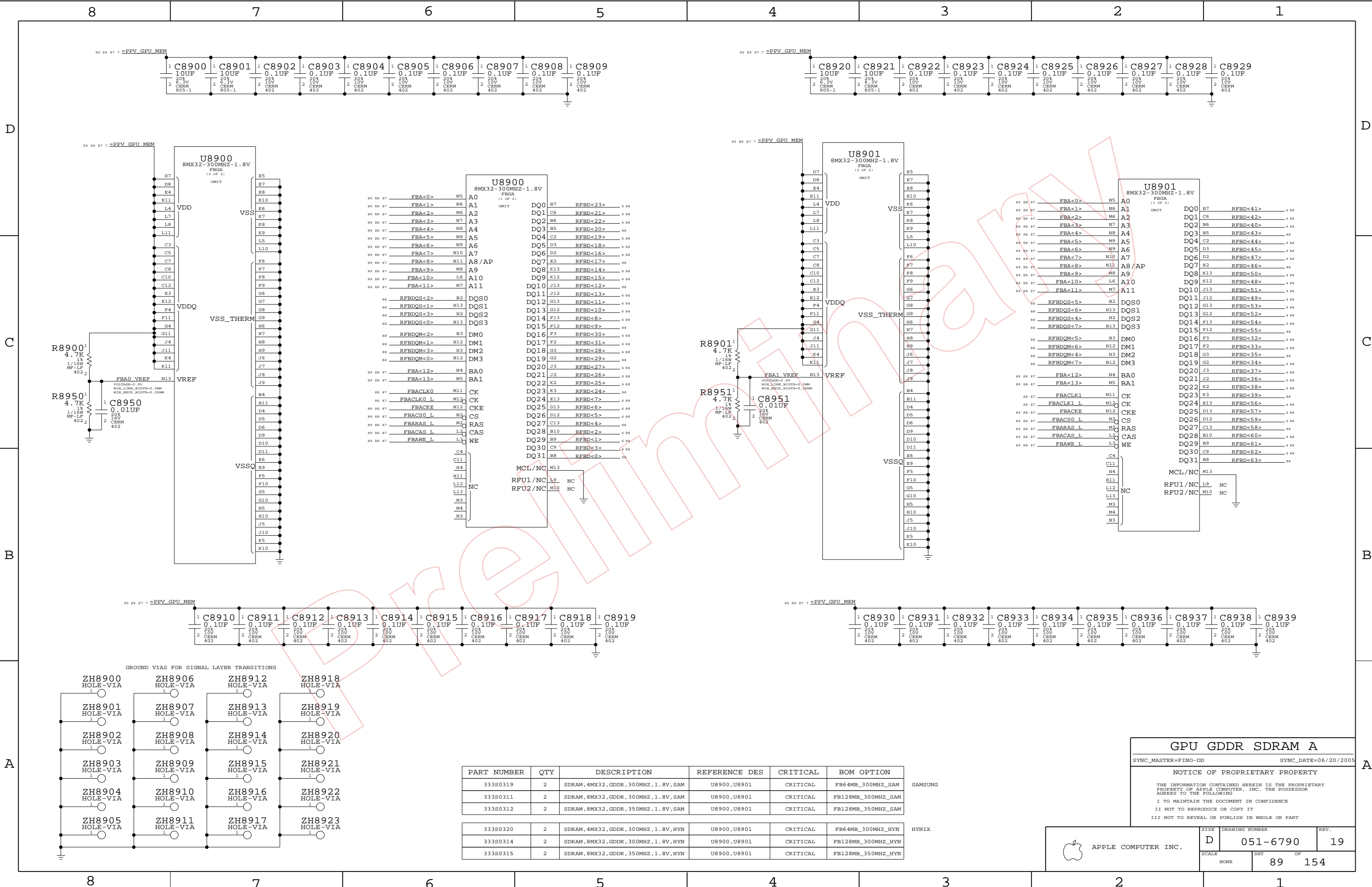
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0319	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB64MB_300MHZ_SAM
333S0311	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_300MHZ_SAM
333S0312	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_350MHZ_SAM
333S0320	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB64MB_300MHZ_HYN
333S0314	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_300MHZ_HYN
333S0315	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_350MHZ_HYN

GPU GDDR SDRAM A

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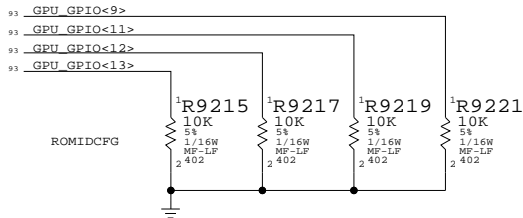
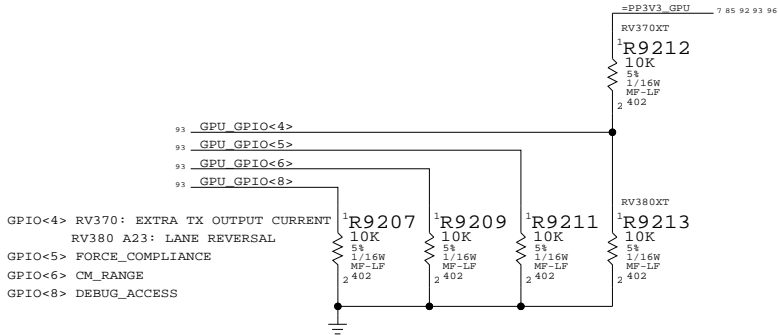
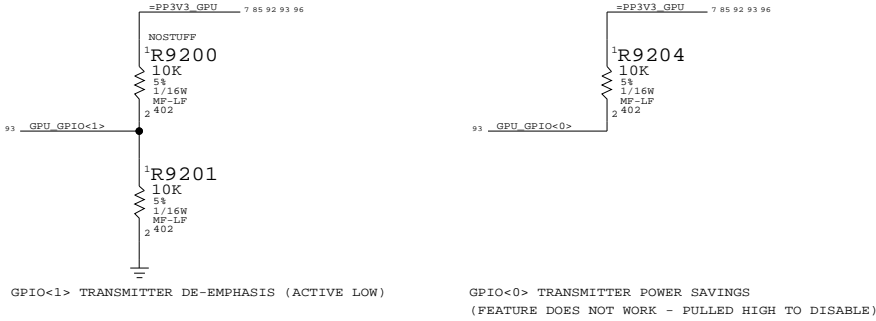
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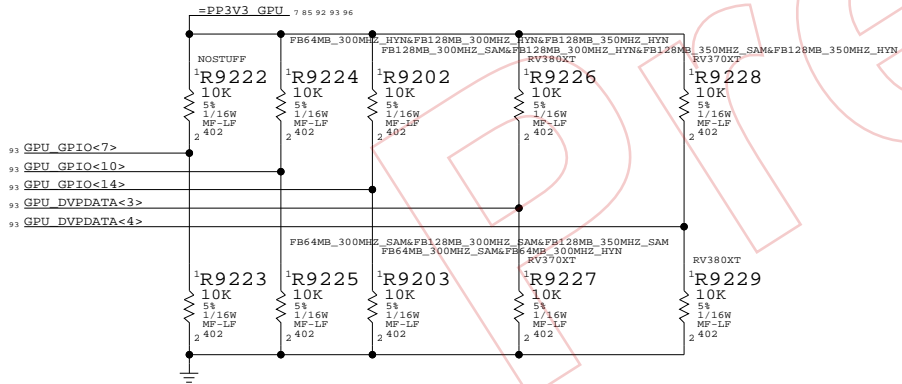
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ATI STRAPS

APPLE GPIOS



MEMORY STRAPS

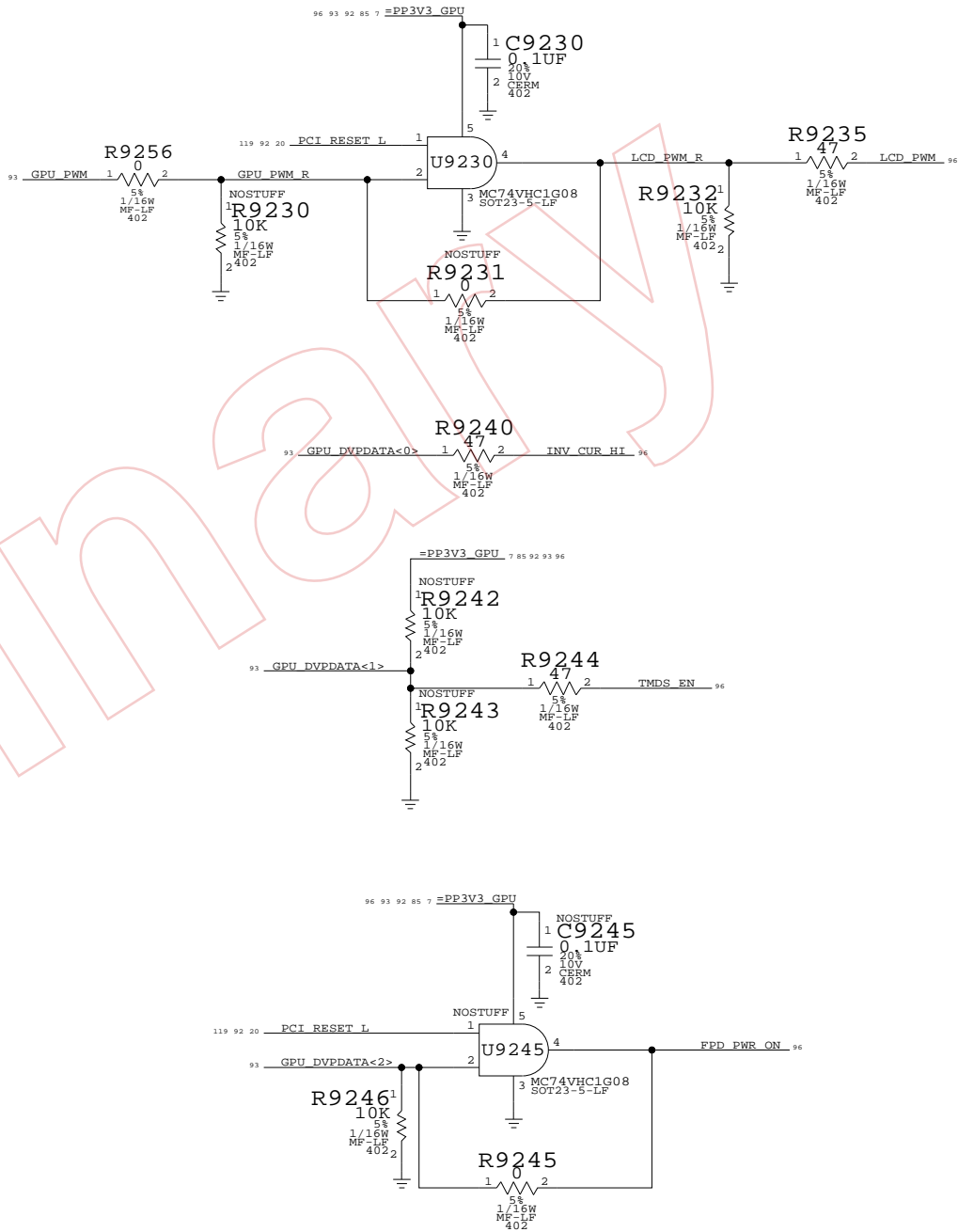


GPIO<7> - MEMORY DIE REVISION
0 - ORIGINAL DIE REVISION
1 - NEW (FUTURE) DIE REV

GPIO<10> - MEMORY VENDOR
0 - SAMSUNG
1 - HYNIX

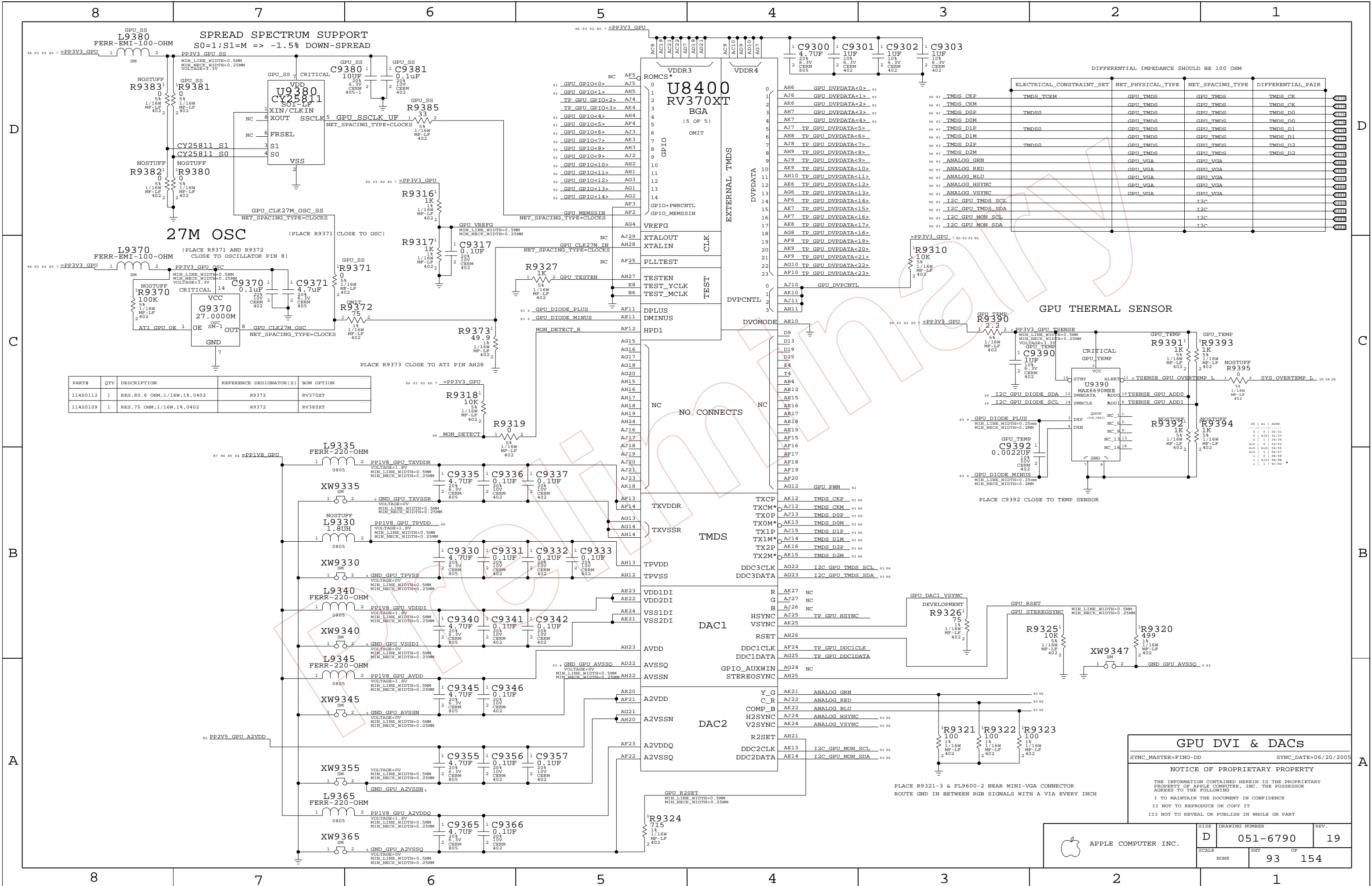
GPIO<14> - MEMORY DENSITY
0 - 4MX32
1 - 8MX32

DVDPDATA<3,4> - SPEED
00 - 325E / 200M
01 - 400E / 300M
10 - 500E / 350M
11 - RESERVED FOR FUTURE USE



GPU Straps		
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	D	051-6790	19
SCALE		SHT	OF
NONE		92	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0112	1	RES,80.6 OHM,1/16W,1%,0402	R9372	RV370XT
114S0109	1	RES,75 OHM,1/16W,1%,0402	R9372	RV380XT

GPU DVI & DACs

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SYNC_DATE=06/20/2005

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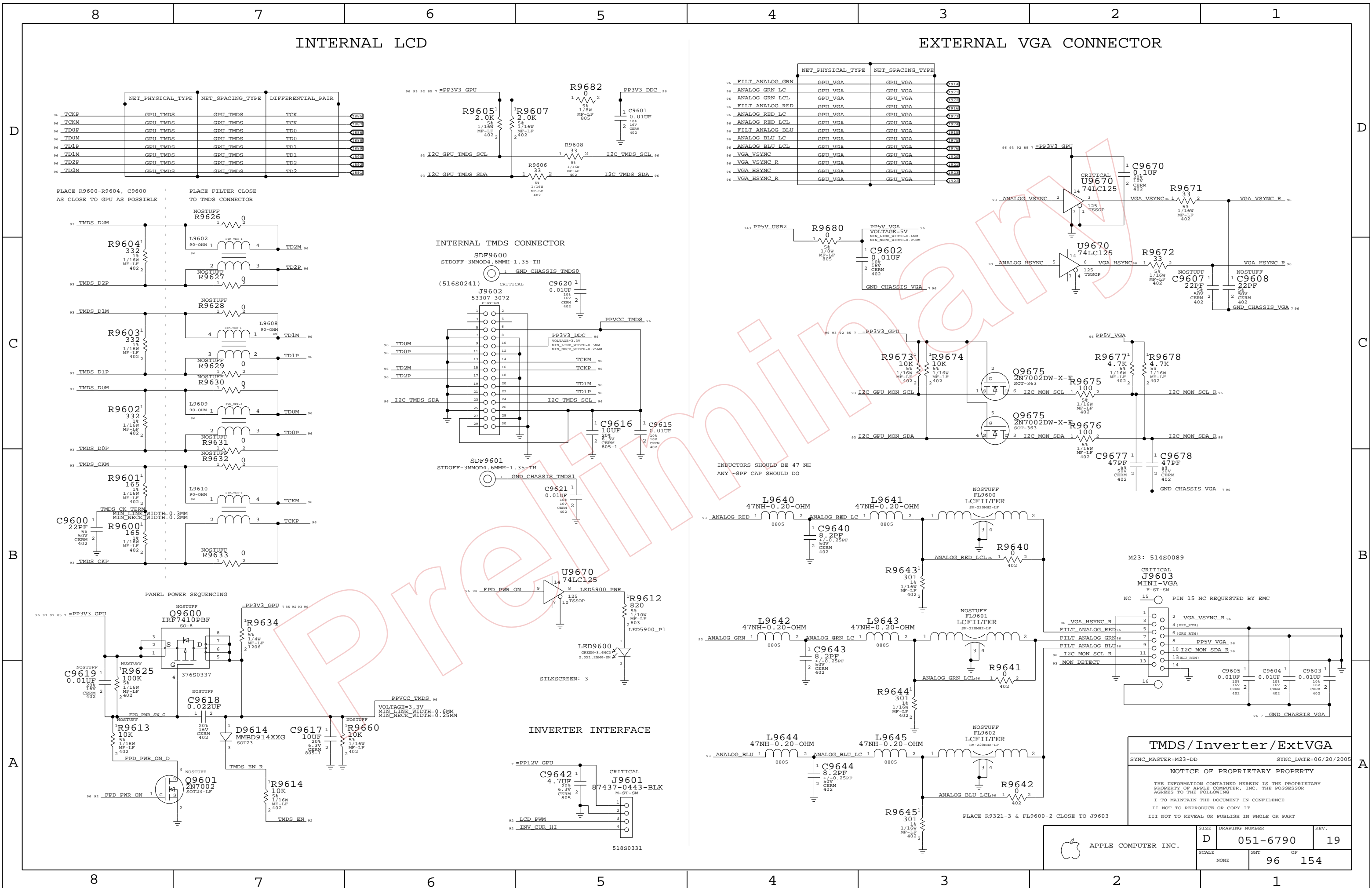
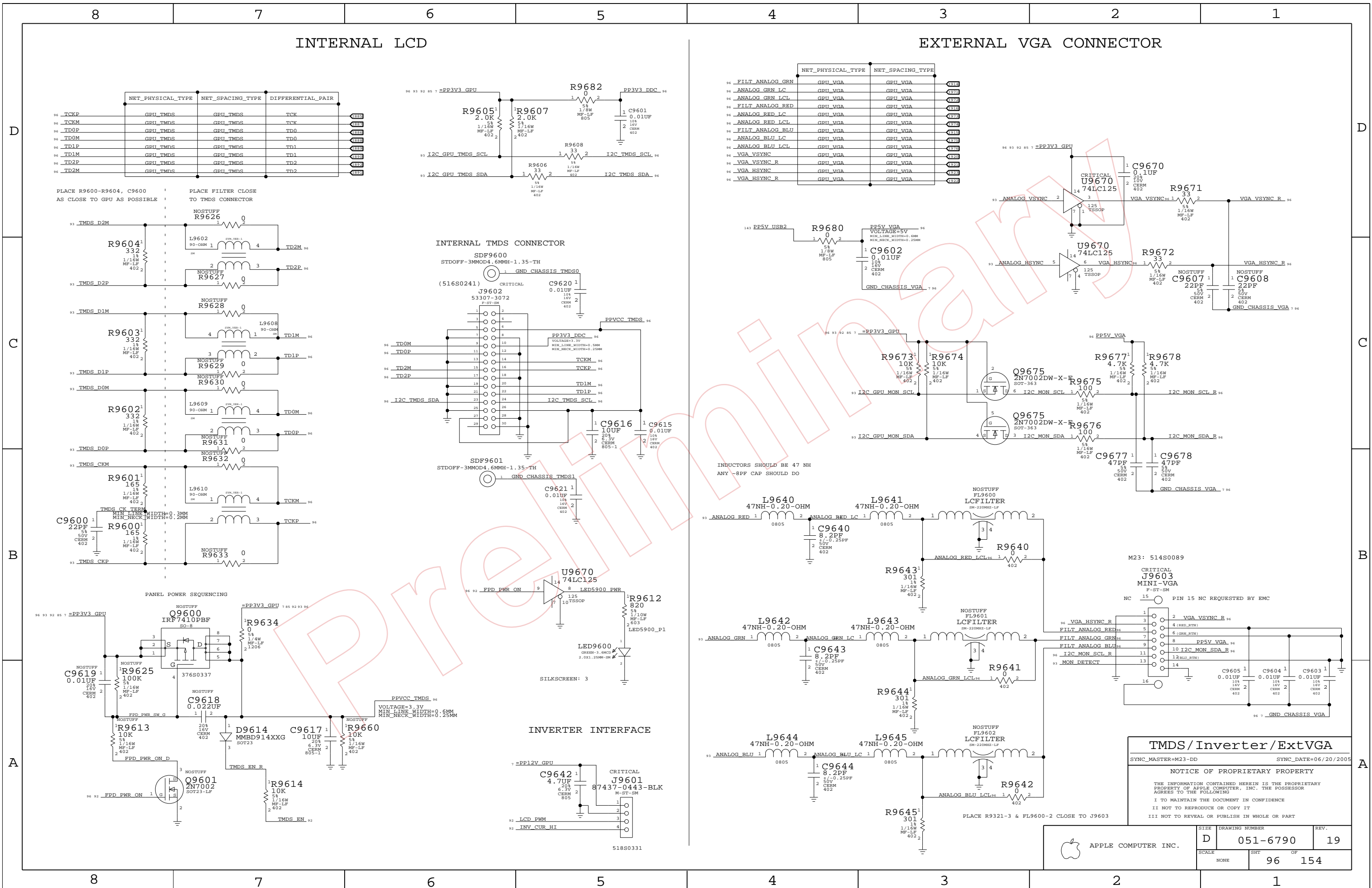
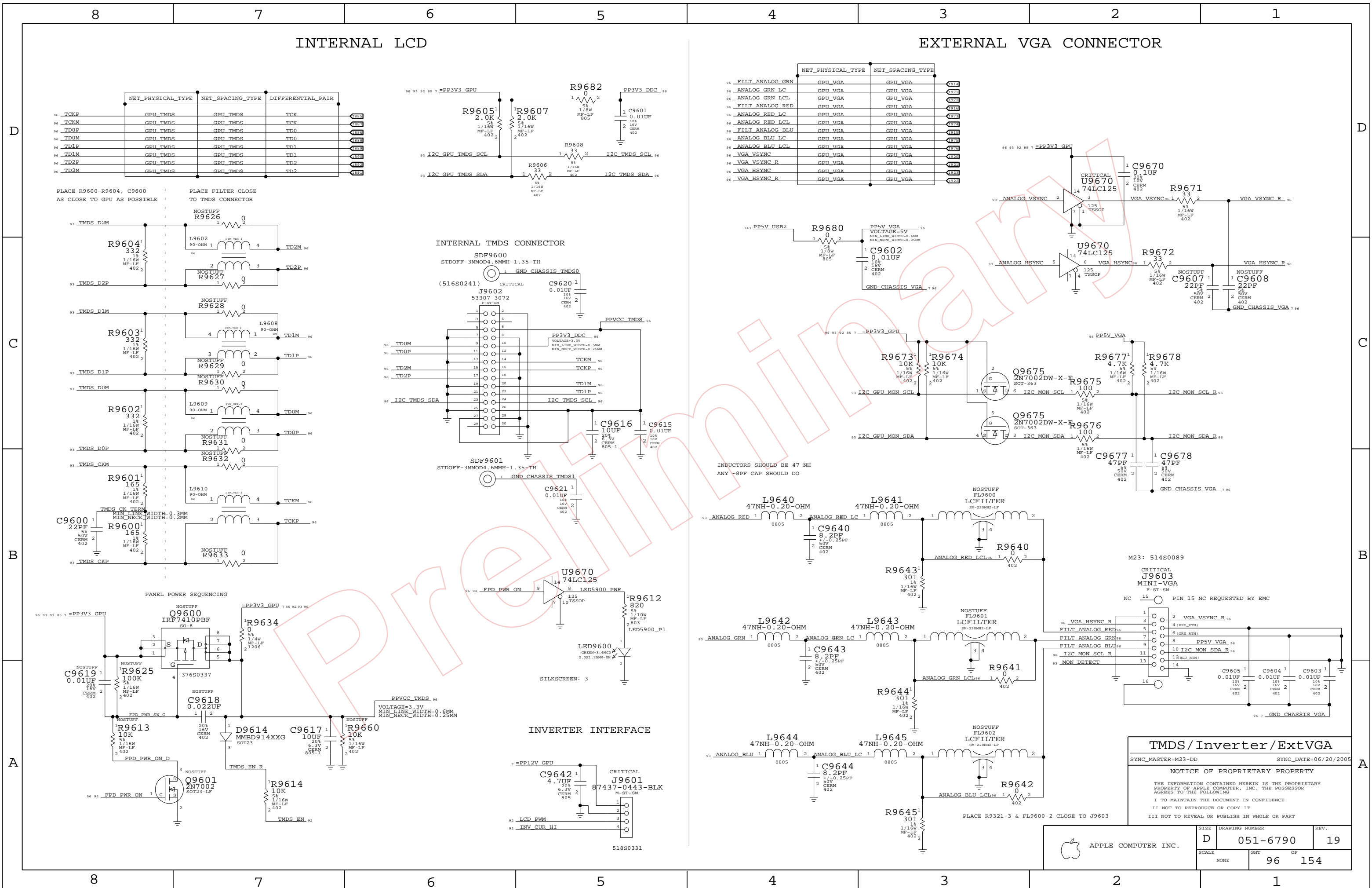
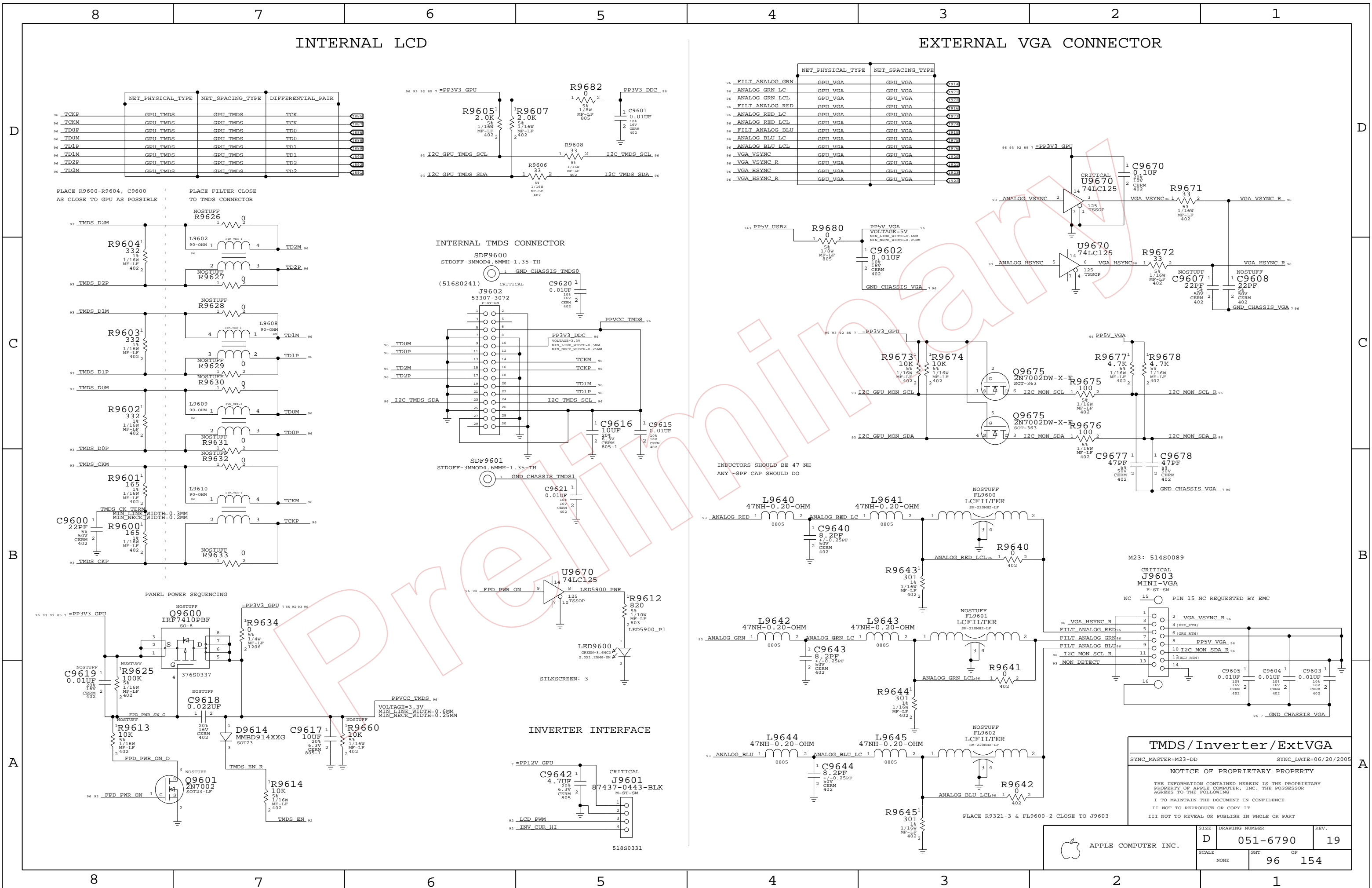
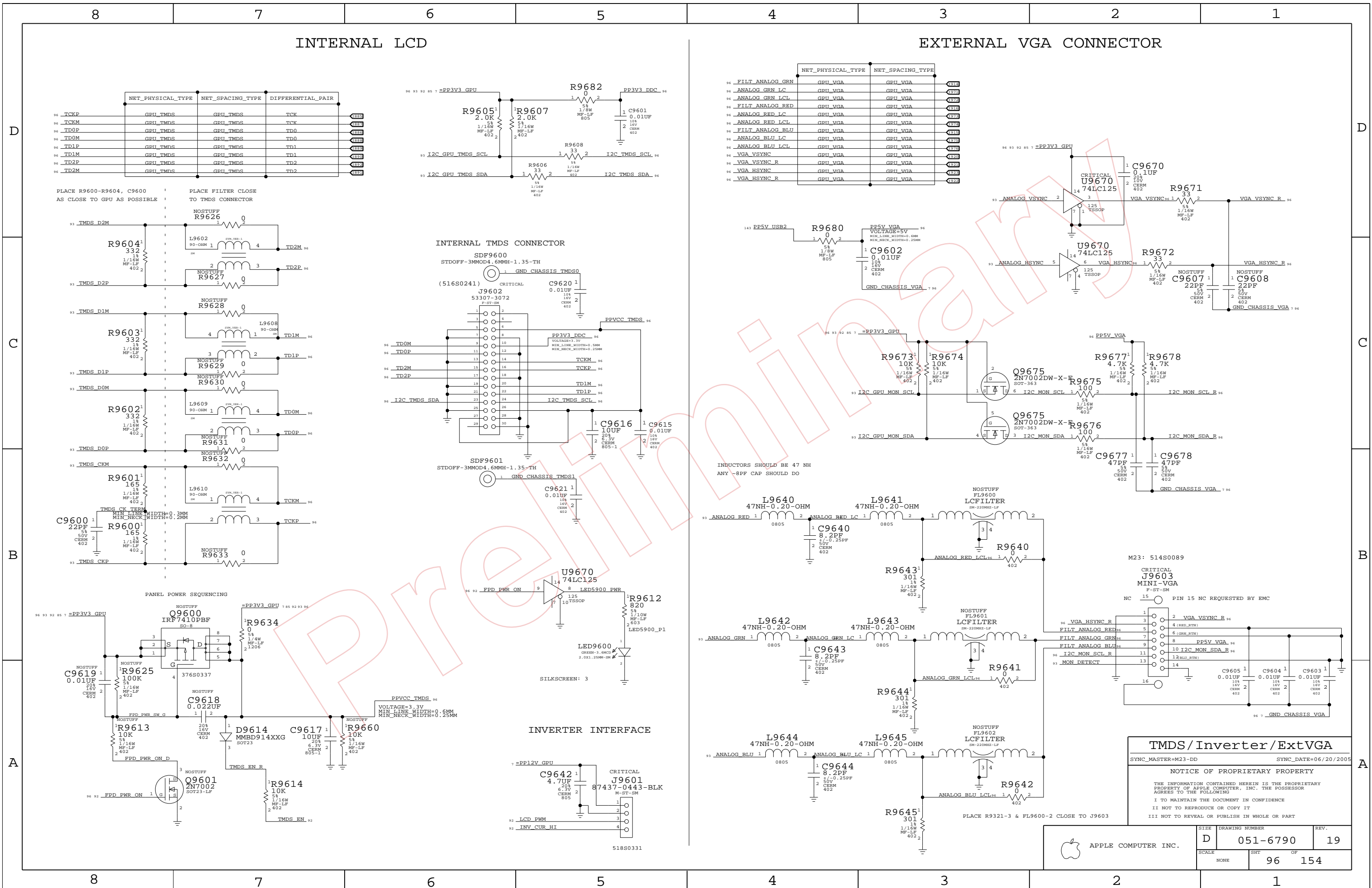
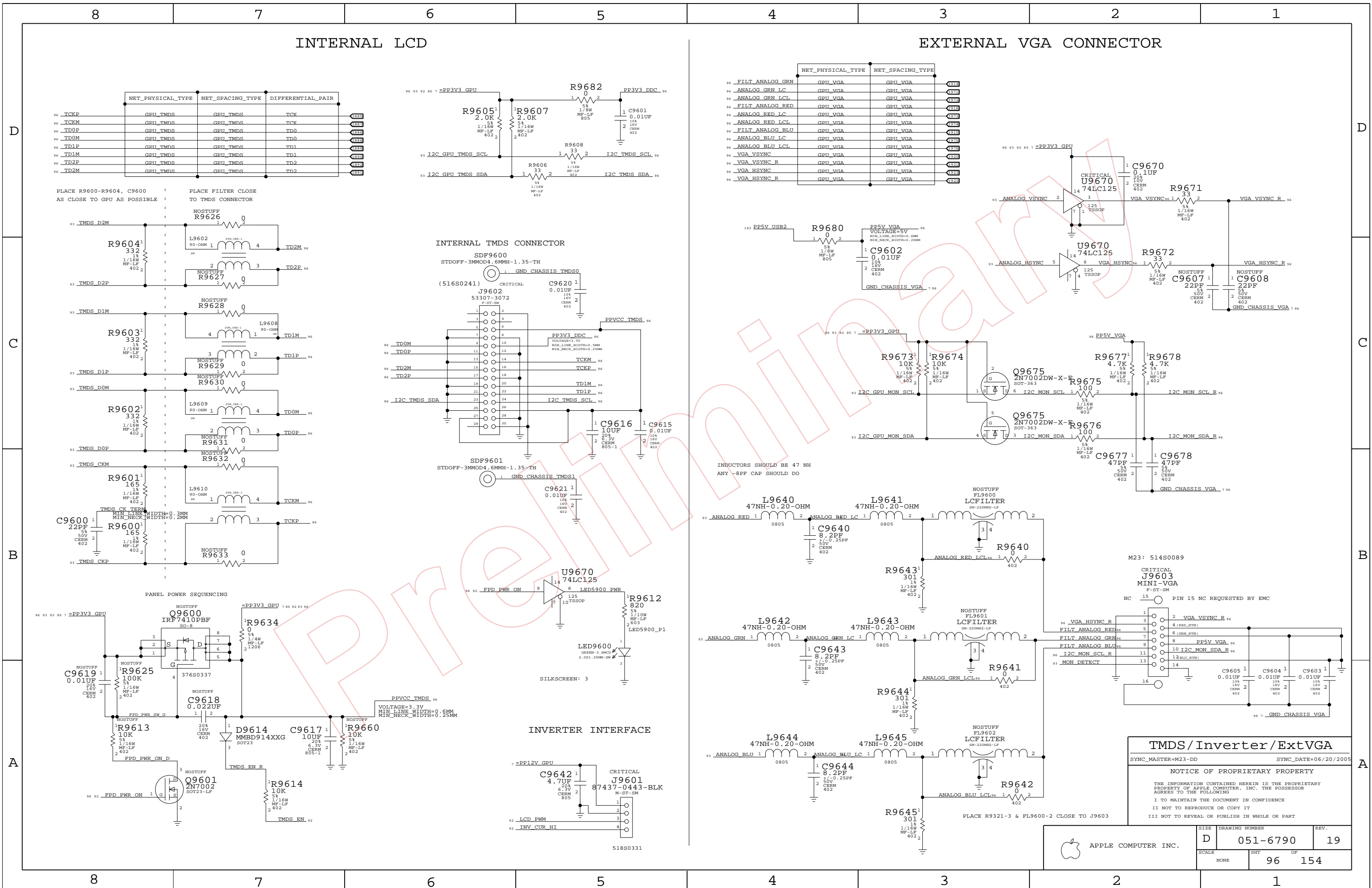
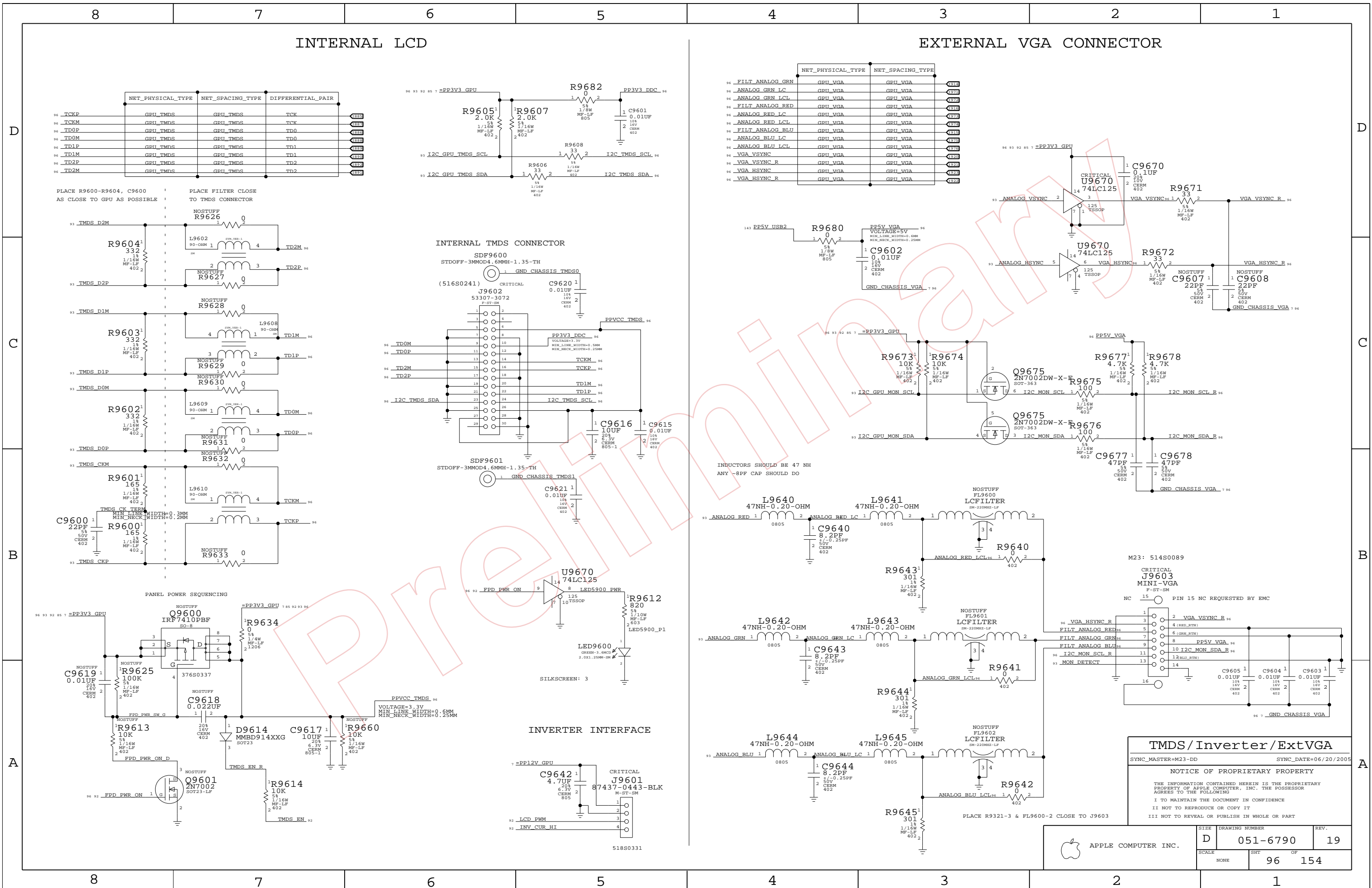
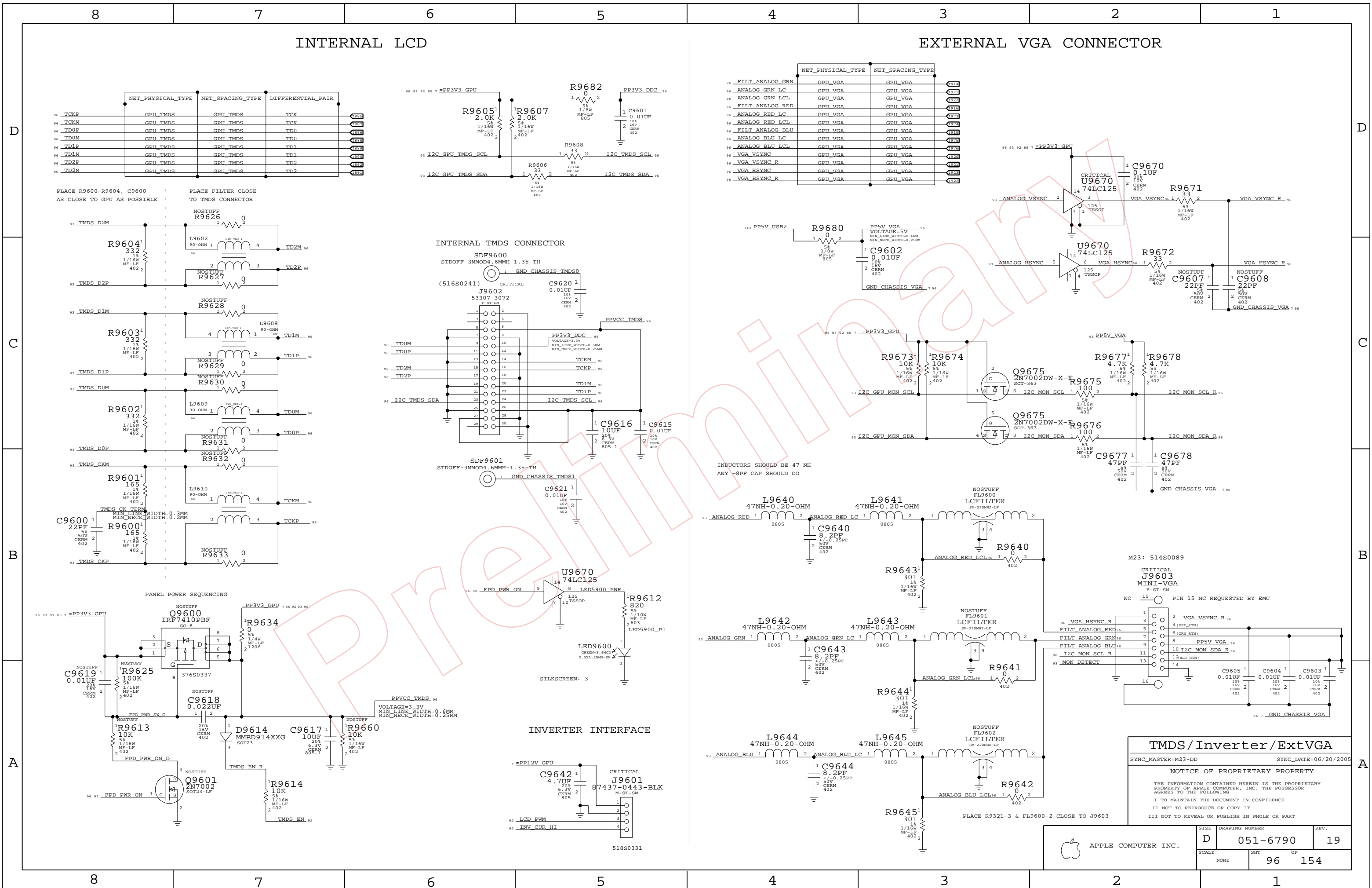
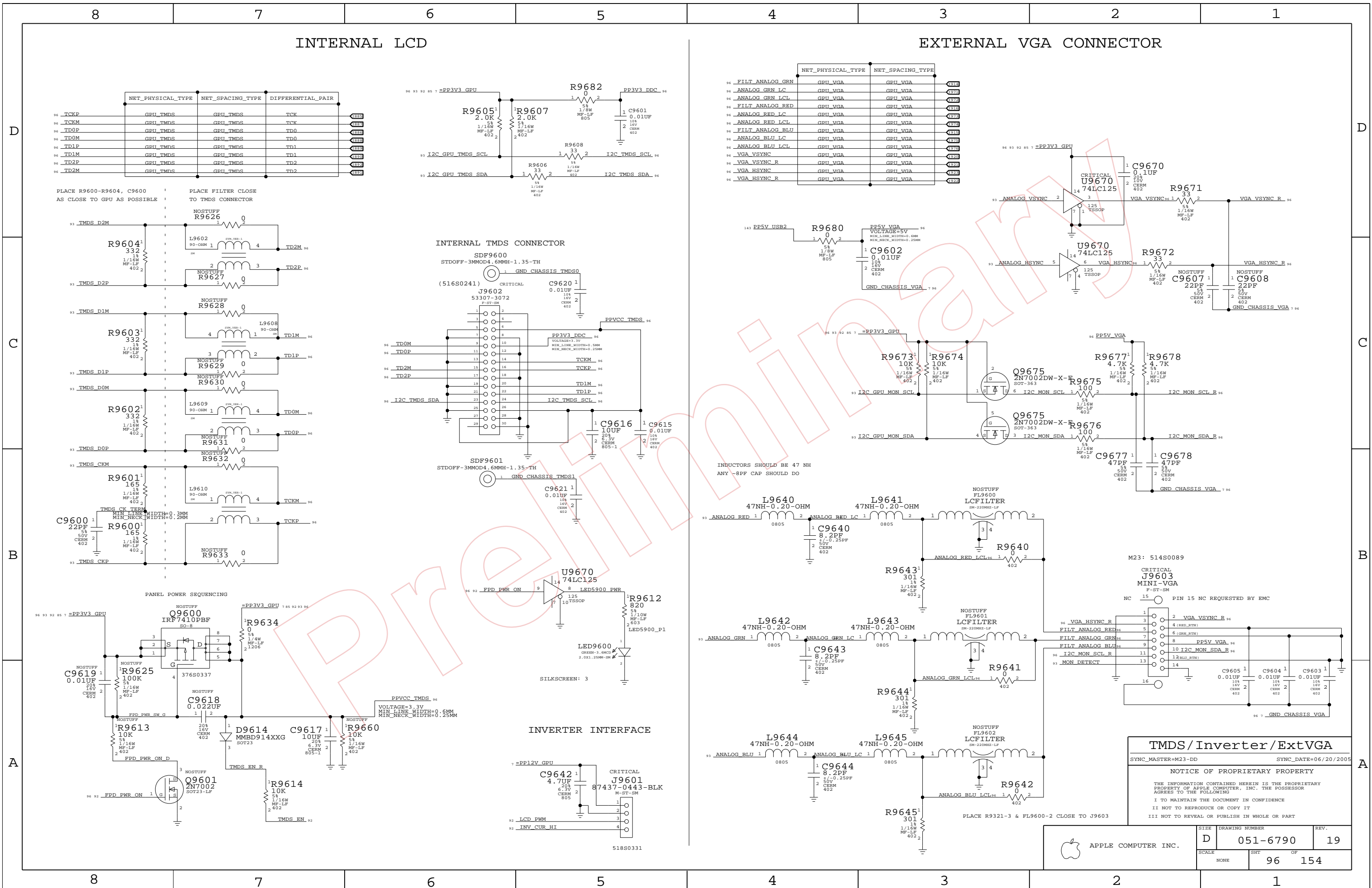
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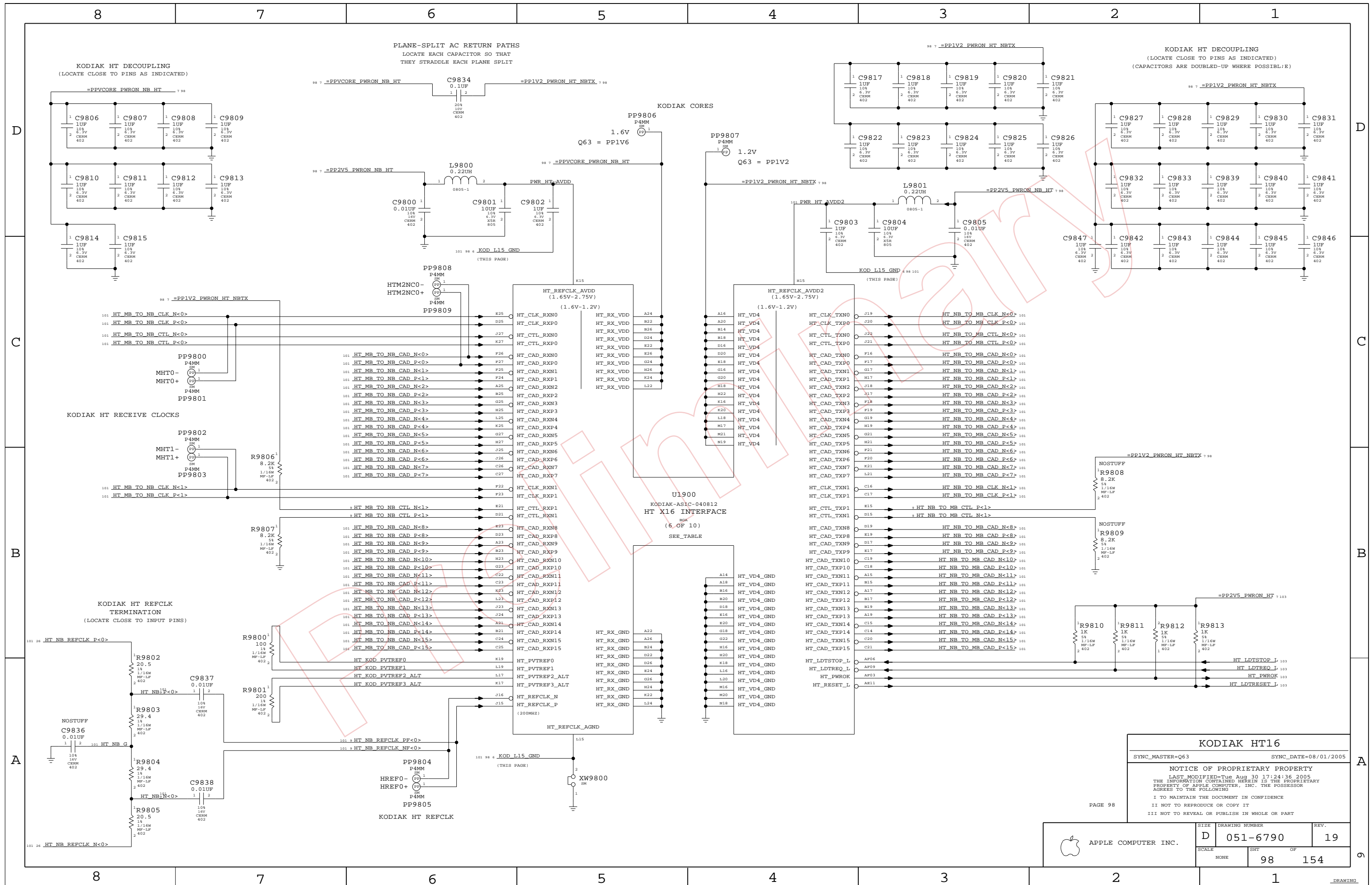
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	D	051-6790	19
SCALE		SHT	OF
NONE		93	154





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SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
PWR_HT_AVDD	0.4MM	0.2MM	2.5
PWR_HT_AVDD2	0.4MM	0.2MM	2.5
KOD_L15_GND	0.4MM	0.2MM	0
HT_NB_G	KEEP DIFF CLOCK FROM BEING A SINGLE XNET		0

HT ALIASES

FINO-ME06/20/2005

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SIZE: D

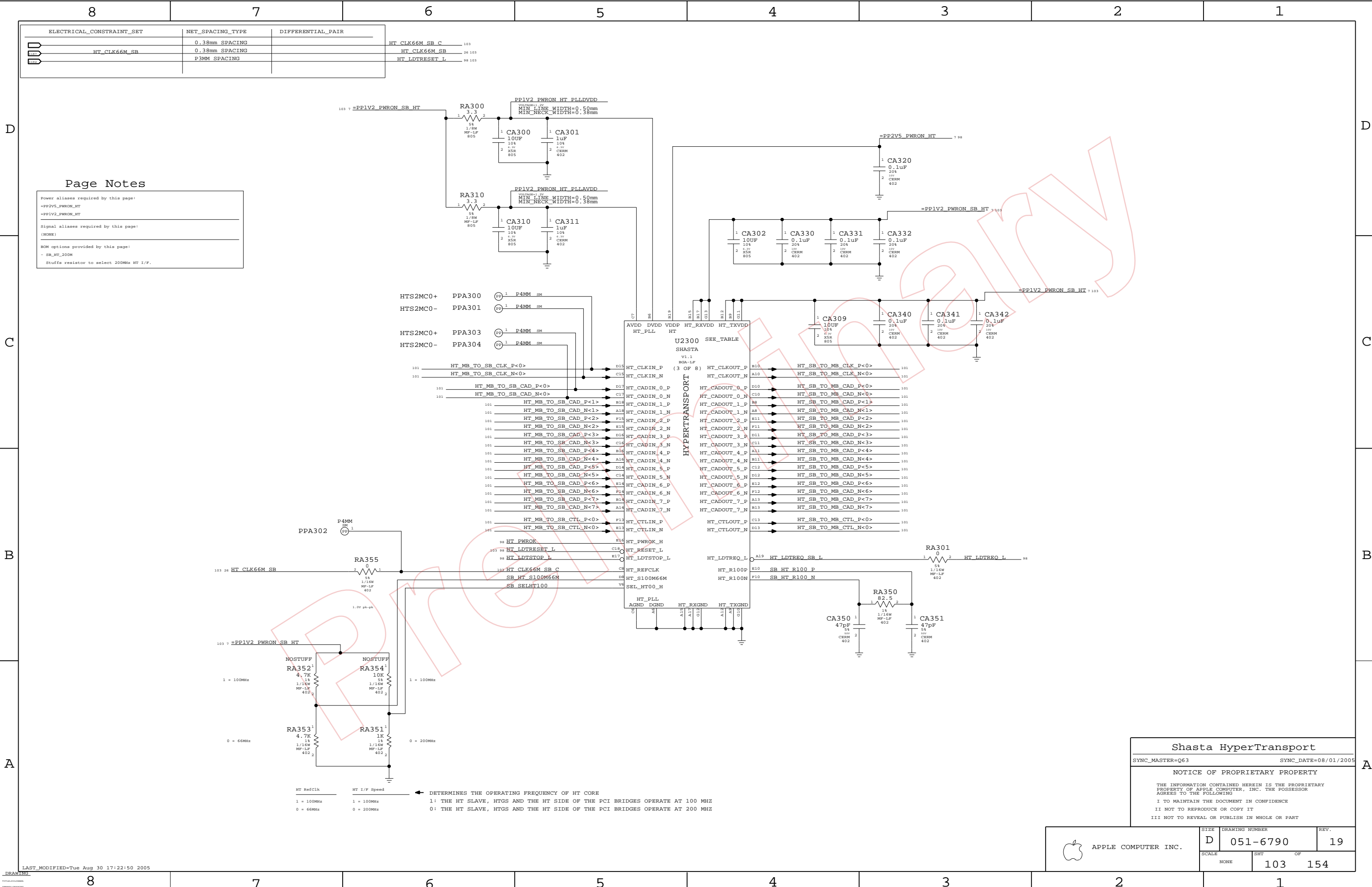
DRAWING NUMBER: 051-6790

REV.: 19

SCALE: NONE

SHT: 101

154



Page Notes

Power aliases required by this page:
=PP2V5_PWRON_HT
=PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M

Stuffs resistor to select 200MHz HT I/F.

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

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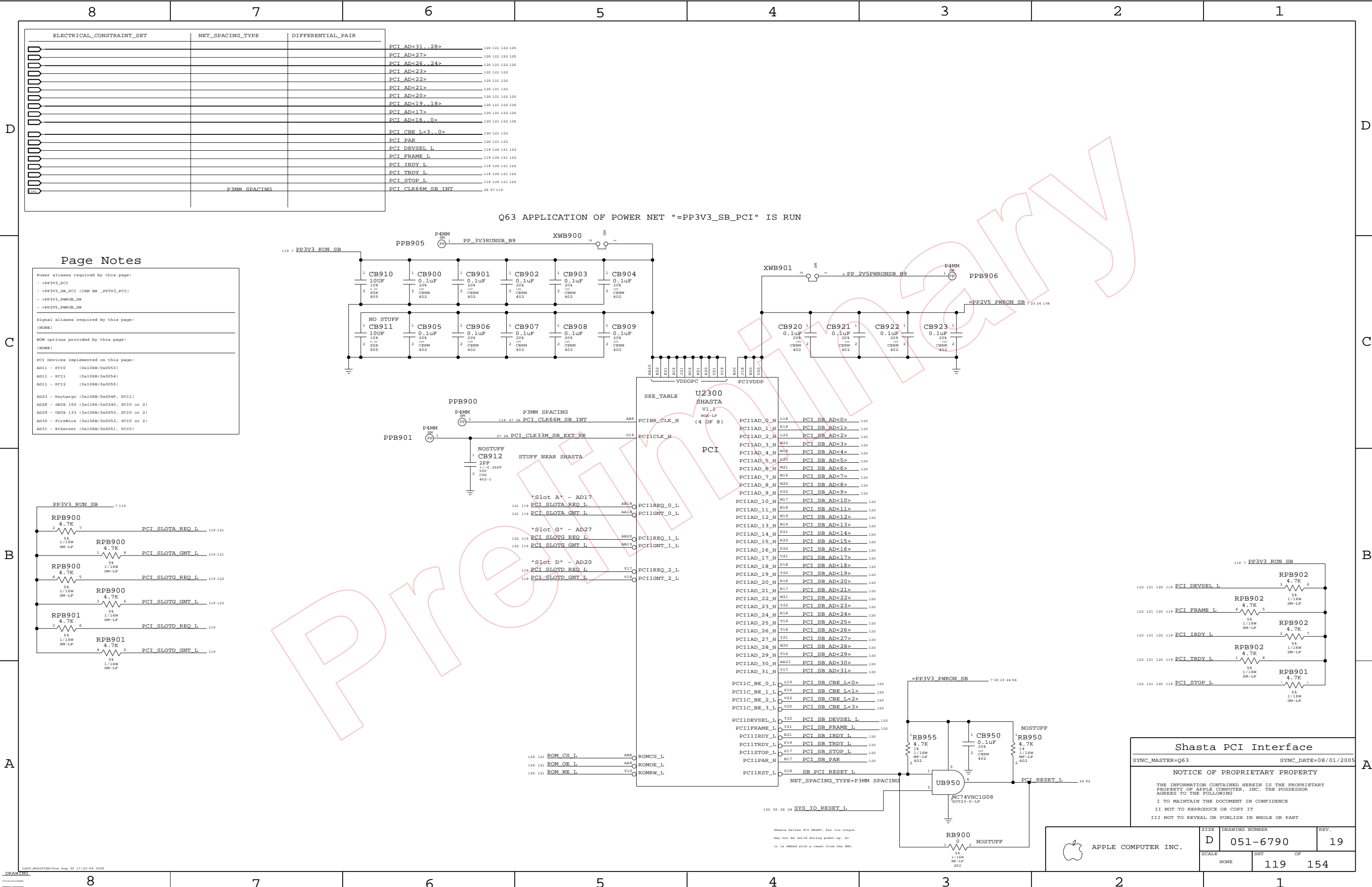
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SIZE	DRAWING NUMBER	REV.
D	051-6790	19
SCALE	SHT	OF
NONE	103	154



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI AD<31..28>		120 121 122 125
PCI AD<27>		120 121 122 125
PCI AD<26..24>		120 121 122 125
PCI AD<23>		120 121 122
PCI AD<22>		120 121 122
PCI AD<21>		120 121 122
PCI AD<20>		120 121 122 125
PCI AD<19..18>		120 121 122 125
PCI AD<17>		120 121 122 125
PCI AD<16..0>		120 121 122 125
PCI CBE L<3..0>		120 121 122
PCI PAR		120 121 122
PCI DEVSEL L		119 120 121 122
PCI FRAME L		119 120 121 122
PCI IRDY L		119 120 121 122
PCI TRDY L		119 120 121 122
PCI STOP L		119 120 121 122
PCI CLK66M_SB_INT		26 27 119
	P3MM SPACING	

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

Page Notes

Power aliases required by this page:
- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

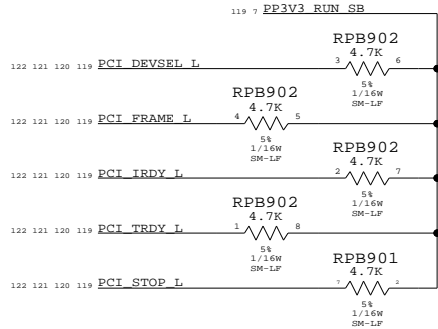
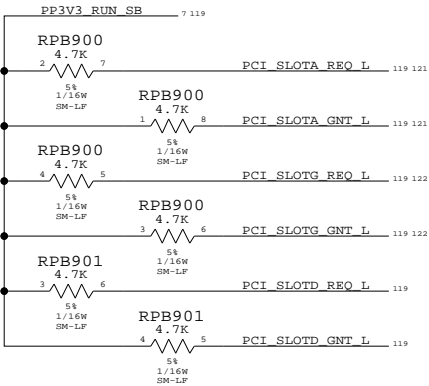
Signal aliases required by this page:
(NONE)

ROM options provided by this page:
(NONE)

PCI Devices implemented on this page:

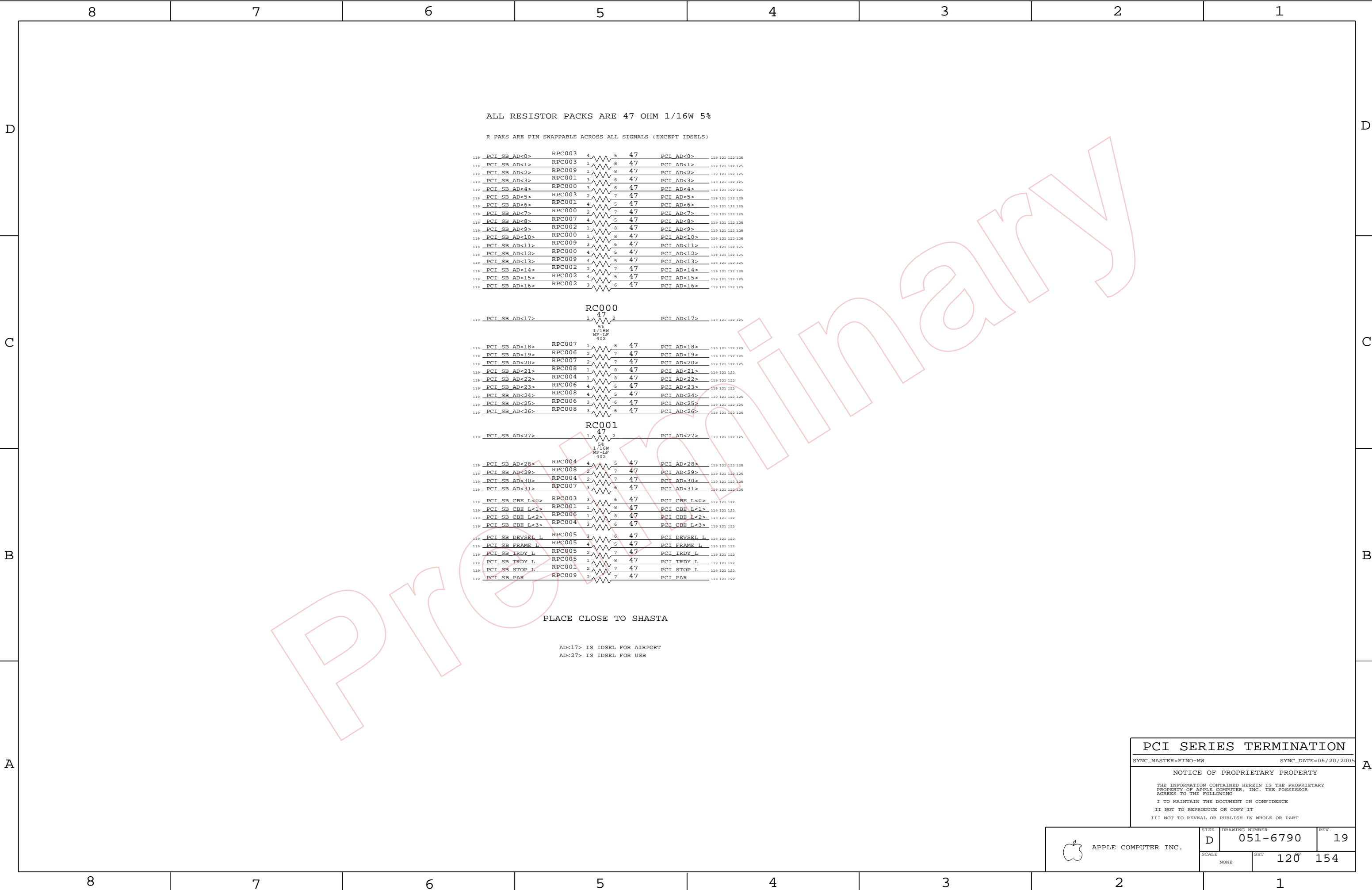
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

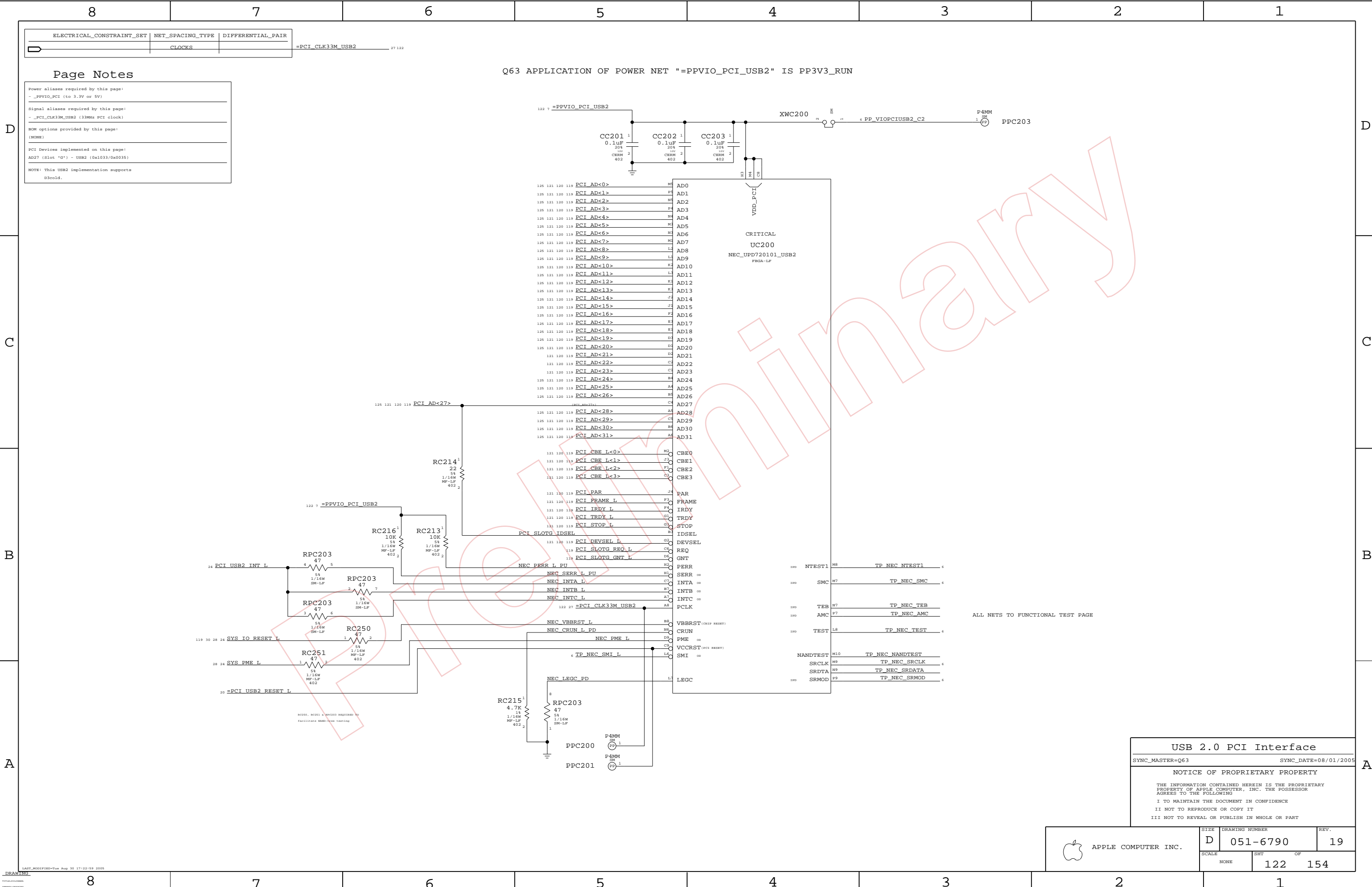
AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)



Shasta PCI Interface	
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005
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APPLE COMPUTER INC.		SIZE	DRAWING NUMBER	REV.
		D	051-6790	19
		SCALE	SHT	OF
		NONE	119	154





ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	
=PCI_CLK33M_USB2		27 122

Page Notes

Power aliases required by this page:

- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:

- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:

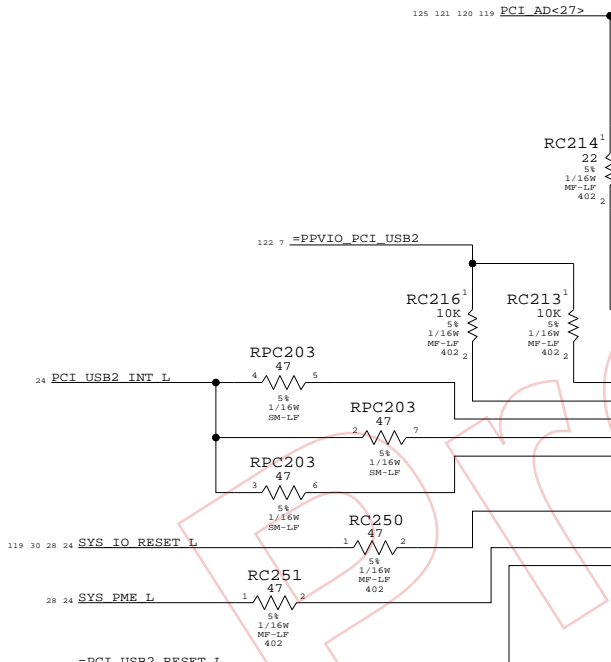
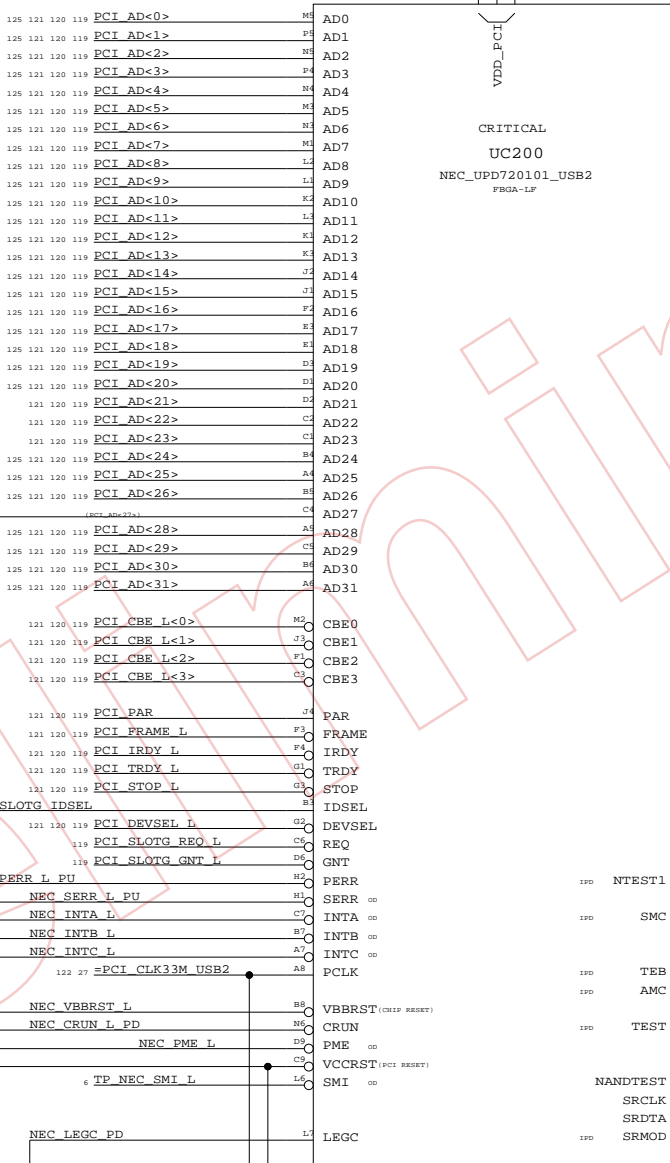
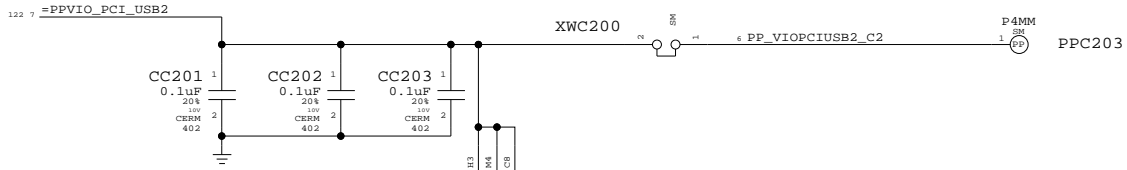
(NONE)

PCI Devices implemented on this page:

AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

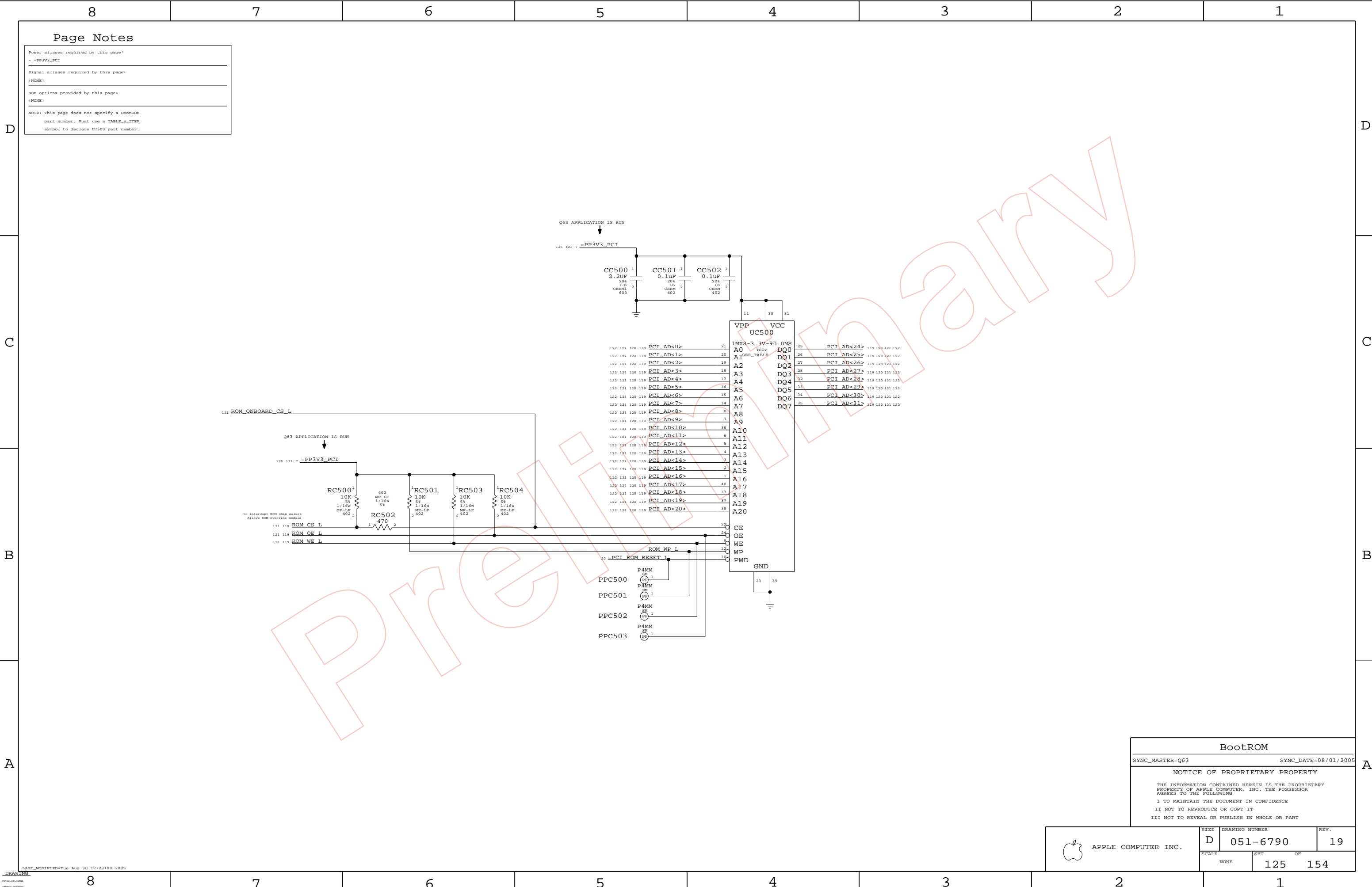


TP_NEC_NTEST1	6
TP_NEC_SMC	6
TP_NEC_TEB	6
TP_NEC_AMC	6
TP_NEC_TEST	6
TP_NEC_NANDTEST	6
TP_NEC_SRCLK	6
TP_NEC_SRDATA	6
TP_NEC_SRMOD	6

ALL NETS TO FUNCTIONAL TEST PAGE

USB 2.0 PCI Interface	
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	OF
NONE		122	154



Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
(NONE)

BCM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7500 part number.

BootROM

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

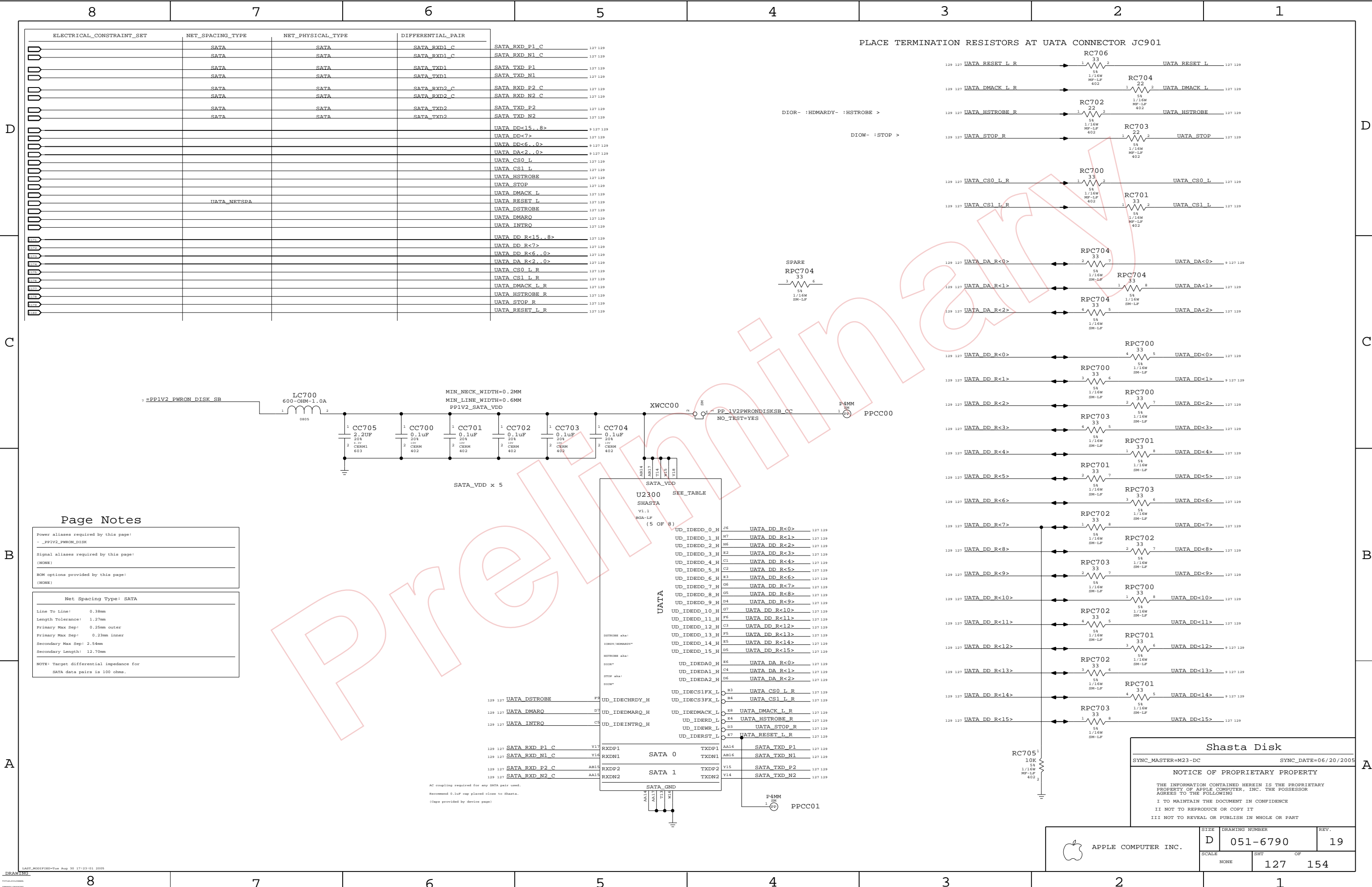
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	OF
NONE		125	154



Page Notes

Power aliases required by this page:
- _PPIV2_PWRON_DISK
Signal aliases required by this page:
(NONE)
ROM options provided by this page:
(NONE)
Net Spacing Type: SATA
Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.25mm outer
Primary Max Sep: 0.23mm inner
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm
NOTE: Target differential impedance for SATA data pairs is 100 ohms.

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

Shasta Disk

SYNC_MASTER=M23-DC SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

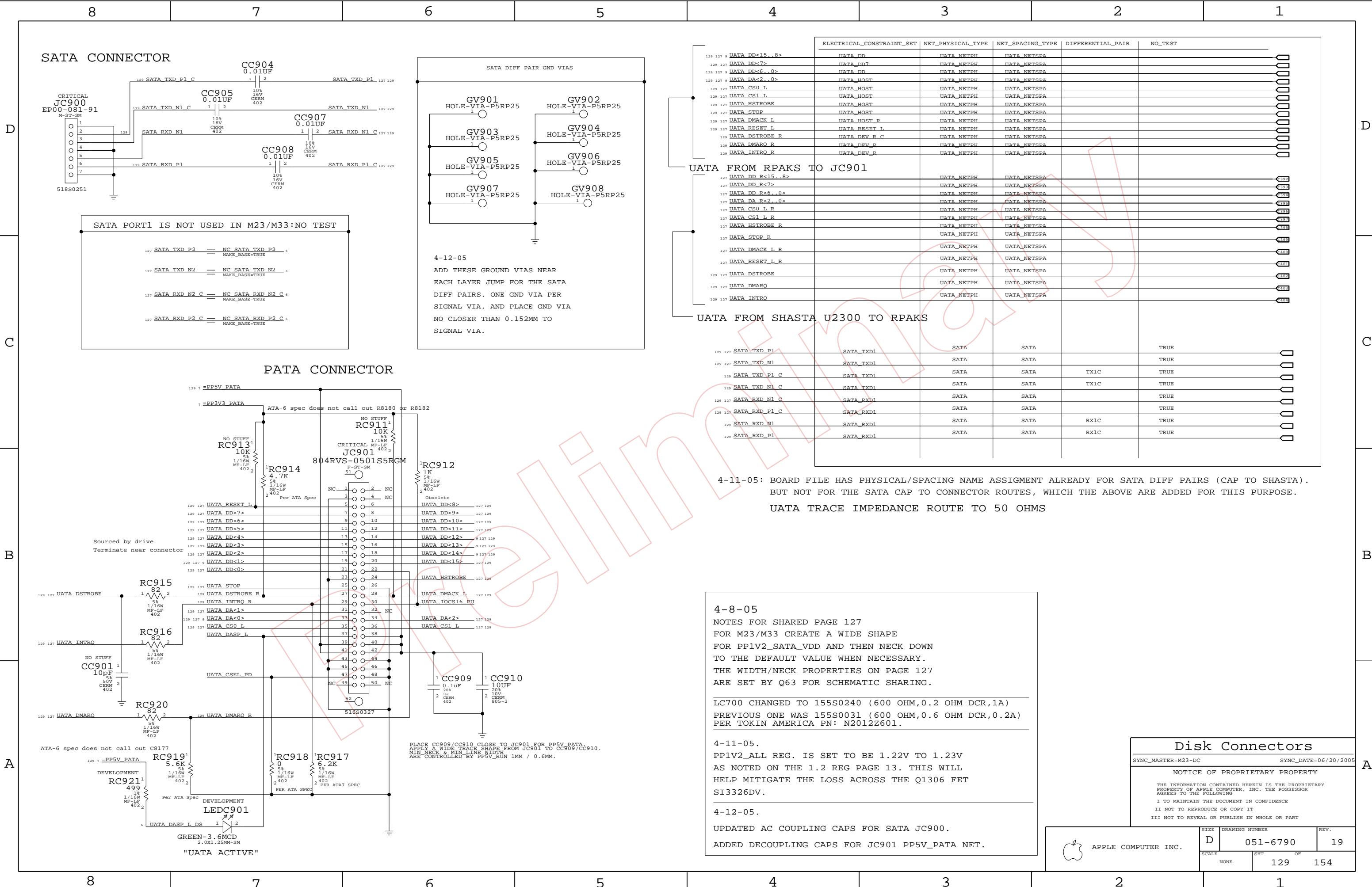
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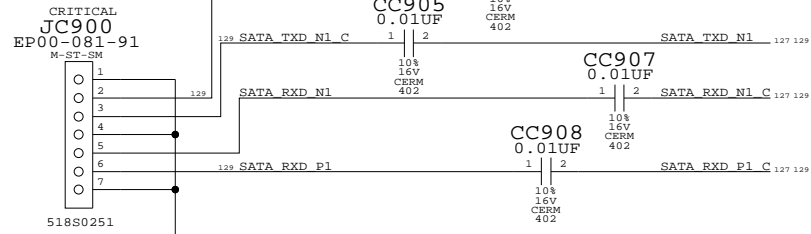
II NOT TO REPRODUCE OR COPY IT

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
	SCALE	SHT	OF
	NONE	127	154



SATA CONNECTOR



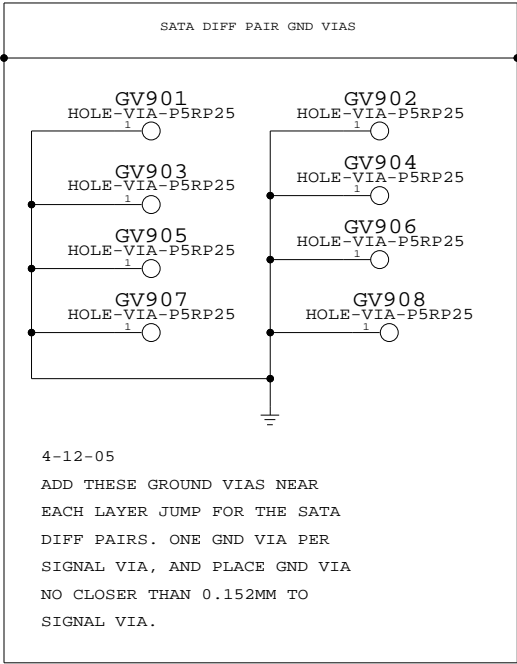
SATA PORT1 IS NOT USED IN M23/M33:NO TEST

127 SATA TXD P2 == NC SATA TXD P2 6
MAKE_BASE=TRUE

127 SATA TXD N2 == NC SATA TXD N2 6
MAKE_BASE=TRUE

127 SATA RXD N2 C == NC SATA RXD N2 C 6
MAKE_BASE=TRUE

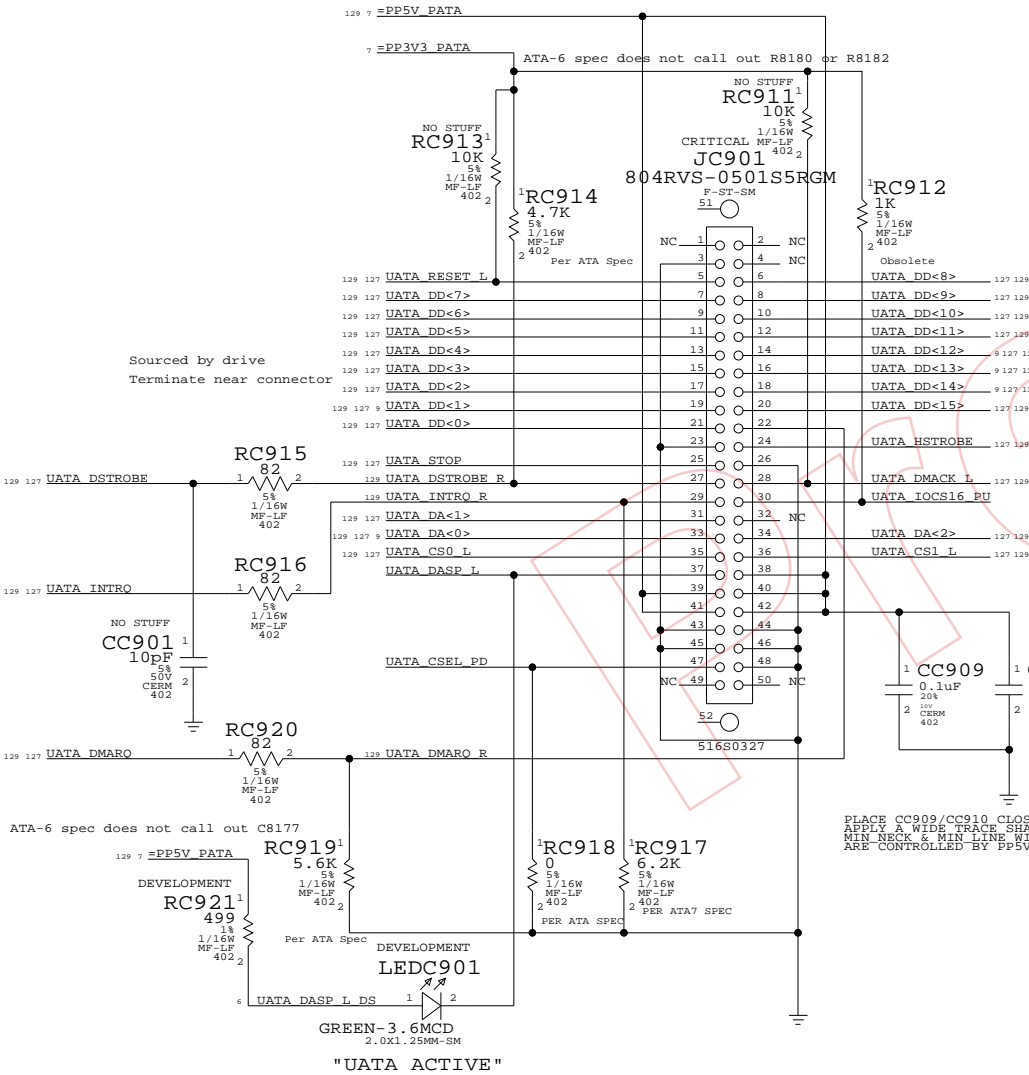
127 SATA RXD P2 C == NC SATA RXD P2 C 6
MAKE_BASE=TRUE



4-12-05

ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA NO CLOSER THAN 0.152MM TO SIGNAL VIA.

PATA CONNECTOR



PLACE CC909/CC910 CLOSE TO JC901 FOR PP5V_PATA. APPLY A WIDE TRACE SHAPE FROM JC901 TO CC909/CC910. MIN NECK & MIN LINE WIDTH ARE CONTROLLED BY PP5V_RUN 1MM / 0.6MM.

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST	
129 127 9	UATA_DD<15..8>	UATA_NETPH	UATA_NETSPA			UATA_DD<15..8>
129 127	UATA_DD<7>	UATA_NETPH	UATA_NETSPA			UATA_DD<7>
129 127 9	UATA_DD<6..0>	UATA_NETPH	UATA_NETSPA			UATA_DD<6..0>
129 127 9	UATA_DA<2..0>	UATA_HOST	UATA_NETSPA			UATA_DA<2..0>
129 127	UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		UATA_CS0_L
129 127	UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		UATA_CS1_L
129 127	UATA_HSTROBE	UATA_HOST	UATA_NETPH	UATA_NETSPA		UATA_HSTROBE
129 127	UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		UATA_STOP
129 127	UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		UATA_DMACK_L
129 127	UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		UATA_RESET_L
129 127	UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		UATA_DSTROBE_R
129 127	UATA_DMARO_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		UATA_DMARO_R
129 127	UATA_INTRO_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		UATA_INTRO_R
129 127	UATA_DD_R<15..8>	UATA_NETPH	UATA_NETSPA			UATA_DD_R<15..8>
129 127	UATA_DD_R<7>	UATA_NETPH	UATA_NETSPA			UATA_DD_R<7>
129 127	UATA_DD_R<6..0>	UATA_NETPH	UATA_NETSPA			UATA_DD_R<6..0>
129 127	UATA_DA_R<2..0>	UATA_NETPH	UATA_NETSPA			UATA_DA_R<2..0>
129 127	UATA_CS0_L_R	UATA_NETPH	UATA_NETSPA			UATA_CS0_L_R
129 127	UATA_CS1_L_R	UATA_NETPH	UATA_NETSPA			UATA_CS1_L_R
129 127	UATA_HSTROBE_R	UATA_NETPH	UATA_NETSPA			UATA_HSTROBE_R
129 127	UATA_STOP_R	UATA_NETPH	UATA_NETSPA			UATA_STOP_R
129 127	UATA_DMACK_L_R	UATA_NETPH	UATA_NETSPA			UATA_DMACK_L_R
129 127	UATA_RESET_L_R	UATA_NETPH	UATA_NETSPA			UATA_RESET_L_R
129 127	UATA_DSTROBE	UATA_NETPH	UATA_NETSPA			UATA_DSTROBE
129 127	UATA_DMARO	UATA_NETPH	UATA_NETSPA			UATA_DMARO
129 127	UATA_INTRO	UATA_NETPH	UATA_NETSPA			UATA_INTRO
129 127	SATA_TXD P1	SATA_TXD1	SATA		TRUE	SATA_TXD P1
129 127	SATA_TXD N1	SATA_TXD1	SATA		TRUE	SATA_TXD N1
129 127	SATA_TXD P1 C	SATA_TXD1	SATA	TX1C	TRUE	SATA_TXD P1 C
129 127	SATA_TXD N1 C	SATA_TXD1	SATA	TX1C	TRUE	SATA_TXD N1 C
129 127	SATA_RXD N1 C	SATA_RXD1	SATA		TRUE	SATA_RXD N1 C
129 127	SATA_RXD P1 C	SATA_RXD1	SATA		TRUE	SATA_RXD P1 C
129 127	SATA_RXD N1	SATA_RXD1	SATA	RX1C	TRUE	SATA_RXD N1
129 127	SATA_RXD P1	SATA_RXD1	SATA	RX1C	TRUE	SATA_RXD P1

UATA FROM RPAKS TO JC901

UATA FROM SHASTA U2300 TO RPAKS

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05

NOTES FOR SHARED PAGE 127

FOR M23/M33 CREATE A WIDE SHAPE FOR PP1V2_SATA_VDD AND THEN NECK DOWN TO THE DEFAULT VALUE WHEN NECESSARY. THE WIDTH/NECK PROPERTIES ON PAGE 127 ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)

PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)

PER TOKIN AMERICA PN: N2012Z601.

4-11-05.

PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL HELP MITIGATE THE LOSS ACROSS THE Q1306 FET SI3326DV.

4-12-05.

UPDATED AC COUPLING CAPS FOR SATA JC900.

ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M23-DC SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-6790 REV. 19

SCALE NONE SHT 129 OF 154



ENET SERIES TERM

SYNC_MASTER=FINO-DC

SYNC_DATE=06/20/2005


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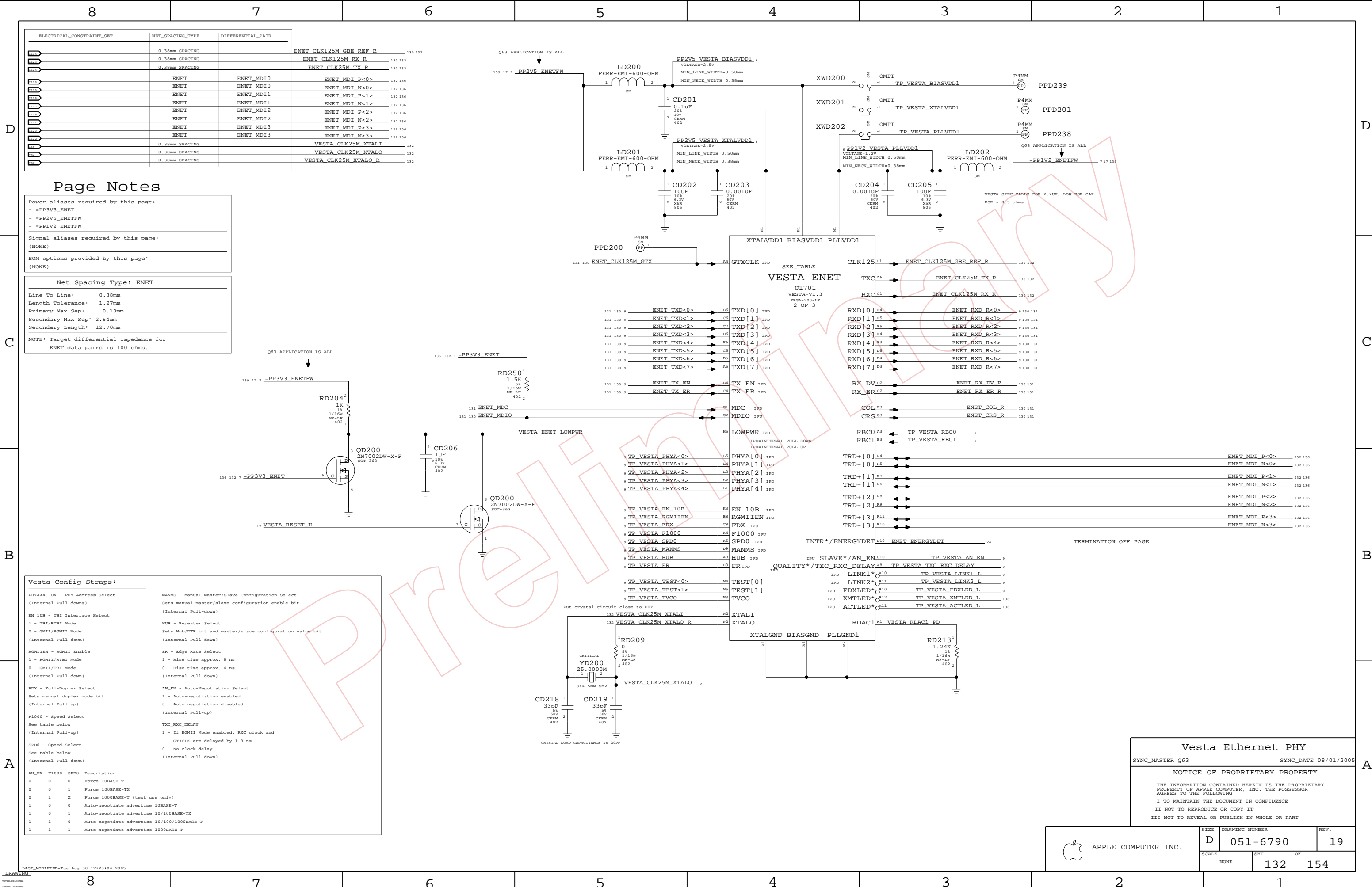
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. 19
	SCALE NONE	SHT 130	154



Page Notes

Power aliases required by this page:

- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select (Internal Pull-downs)
EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode (Internal Pull-down)
RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode (Internal Pull-down)
FDX - Full-Duplex Select
Sets manual duplex mode bit (Internal Pull-up)
F1000 - Speed Select
See table below (Internal Pull-up)
SPD0 - Speed Select
See table below (Internal Pull-down)
AN_EN F1000 SPD0 Description
0 0 0 Force 10BASE-T
0 0 1 Force 100BASE-TX
0 1 X Force 1000BASE-T (test use only)
1 0 0 Auto-negotiate advertise 10BASE-T
1 0 1 Auto-negotiate advertise 10/100BASE-TX
1 1 0 Auto-negotiate advertise 10/100/1000BASE-T
1 1 1 Auto-negotiate advertise 1000BASE-T

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit (Internal Pull-down)
HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit (Internal Pull-down)
ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns (Internal Pull-down)
AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled (Internal Pull-up)
TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay (Internal Pull-down)

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

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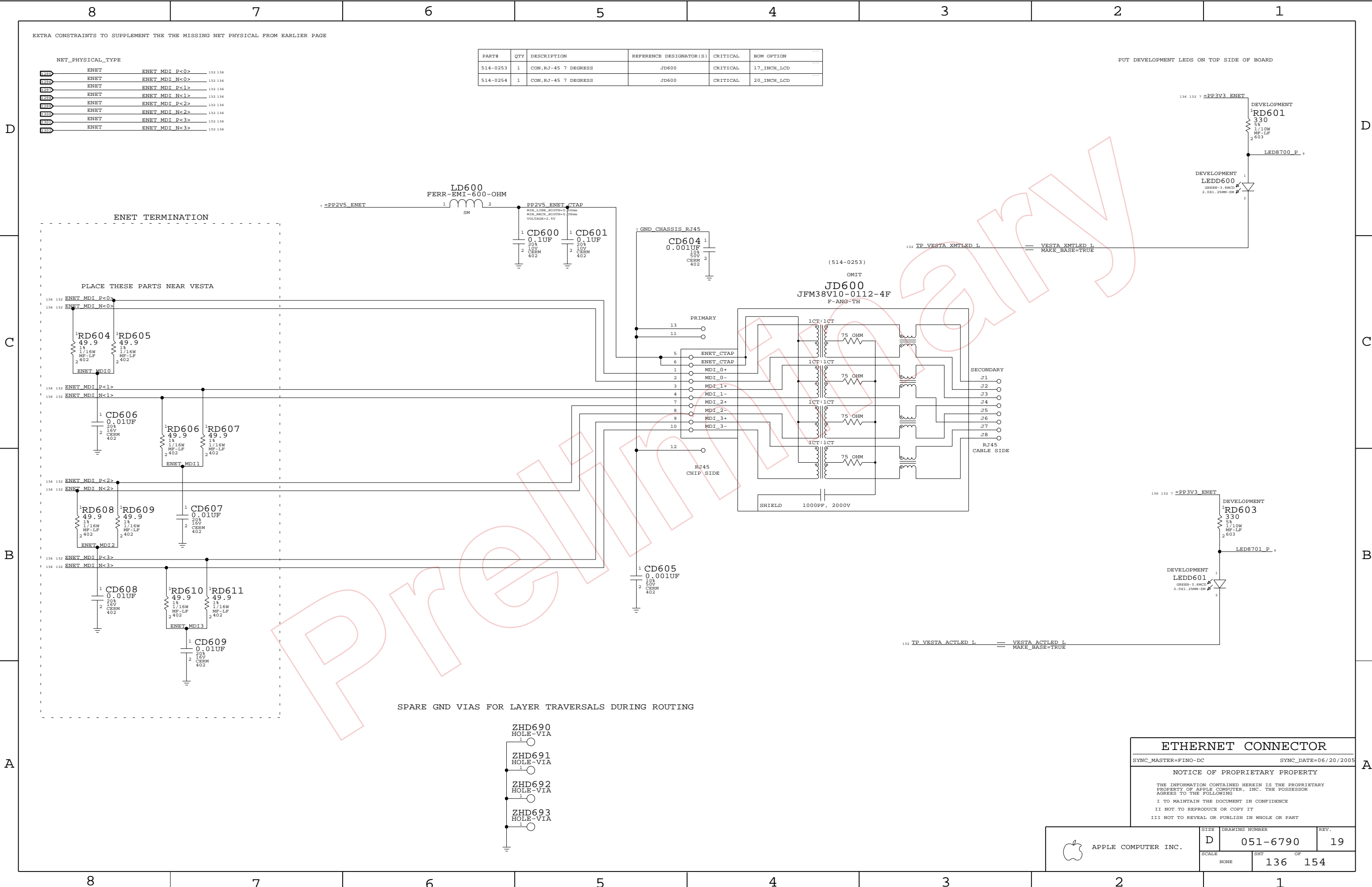


APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6790 19

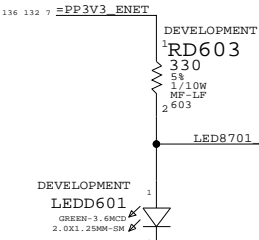
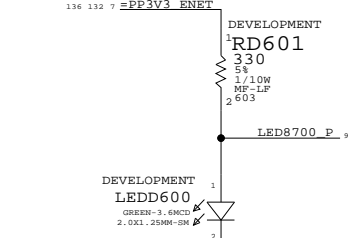
SCALE NONE SHT OF 132 154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

NET_PHYSICAL_TYPE		
ENET	ENET MDI P<0>	132 136
ENET	ENET MDI N<0>	132 136
ENET	ENET MDI P<1>	132 136
ENET	ENET MDI N<1>	132 136
ENET	ENET MDI P<2>	132 136
ENET	ENET MDI N<2>	132 136
ENET	ENET MDI P<3>	132 136
ENET	ENET MDI N<3>	132 136

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD



ETHERNET CONNECTOR	
SYNC_MASTER=FINO-DC	SYNC_DATE=06/20/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	OF
NONE		136	154

D

C

```
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW
```

BOM options provided by this page:

- VESTA_DS_ONLY_EN0
If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

A

```
FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)
```

DRAWING



C

R

 λ

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER		REV.
	D	051-6790		19
	SCALE	NONE	SHT	OF
			139	154



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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D	051-6790
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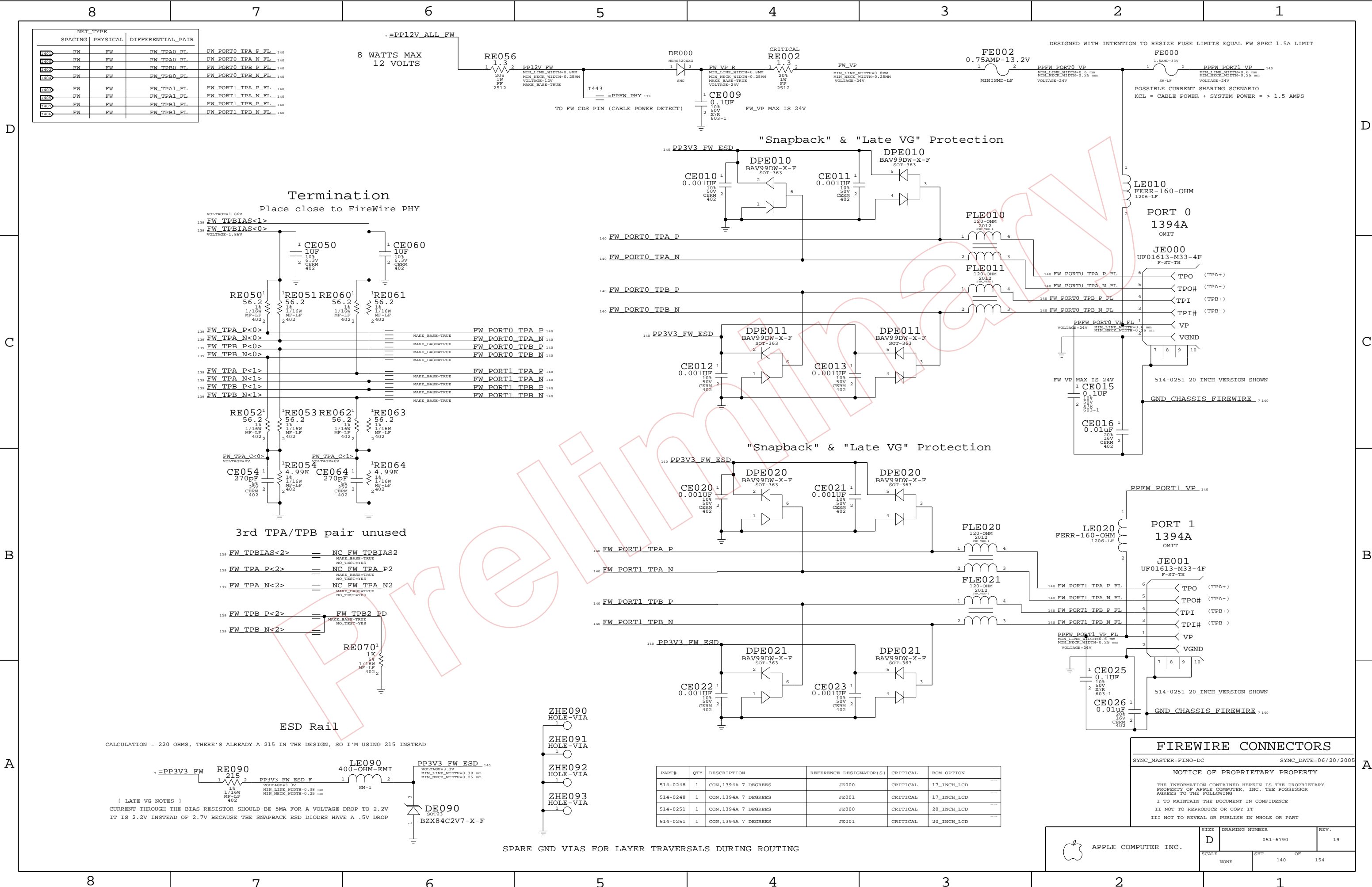
051	0750
-----	------

SCALE	SHA
NONE	120

	139	154
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1

LAST_MODIFIED= Tue Aug 30 17:23:07 2005



Page Notes

Power aliases required by this page:

- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

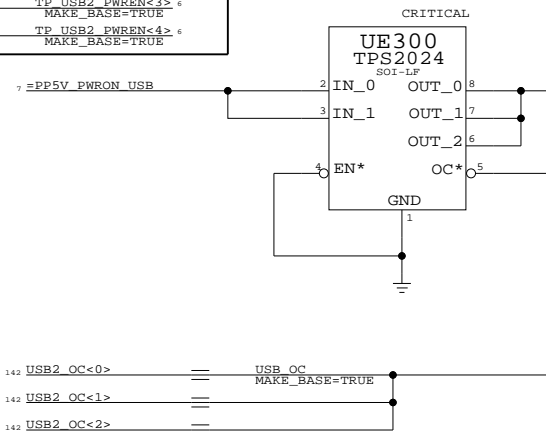
BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

142 USB2_PWREN<0>	==	TP_USB2_PWREN<0>	6
142 USB2_PWREN<1>	==	TP_USB2_PWREN<1>	6
142 USB2_PWREN<2>	==	TP_USB2_PWREN<2>	6
142 USB2_PWREN<3>	==	TP_USB2_PWREN<3>	6
142 USB2_PWREN<4>	==	TP_USB2_PWREN<4>	6

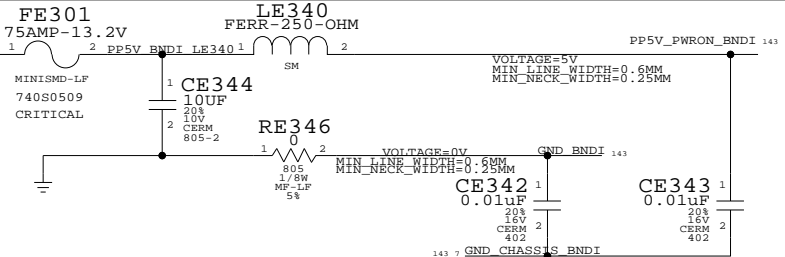
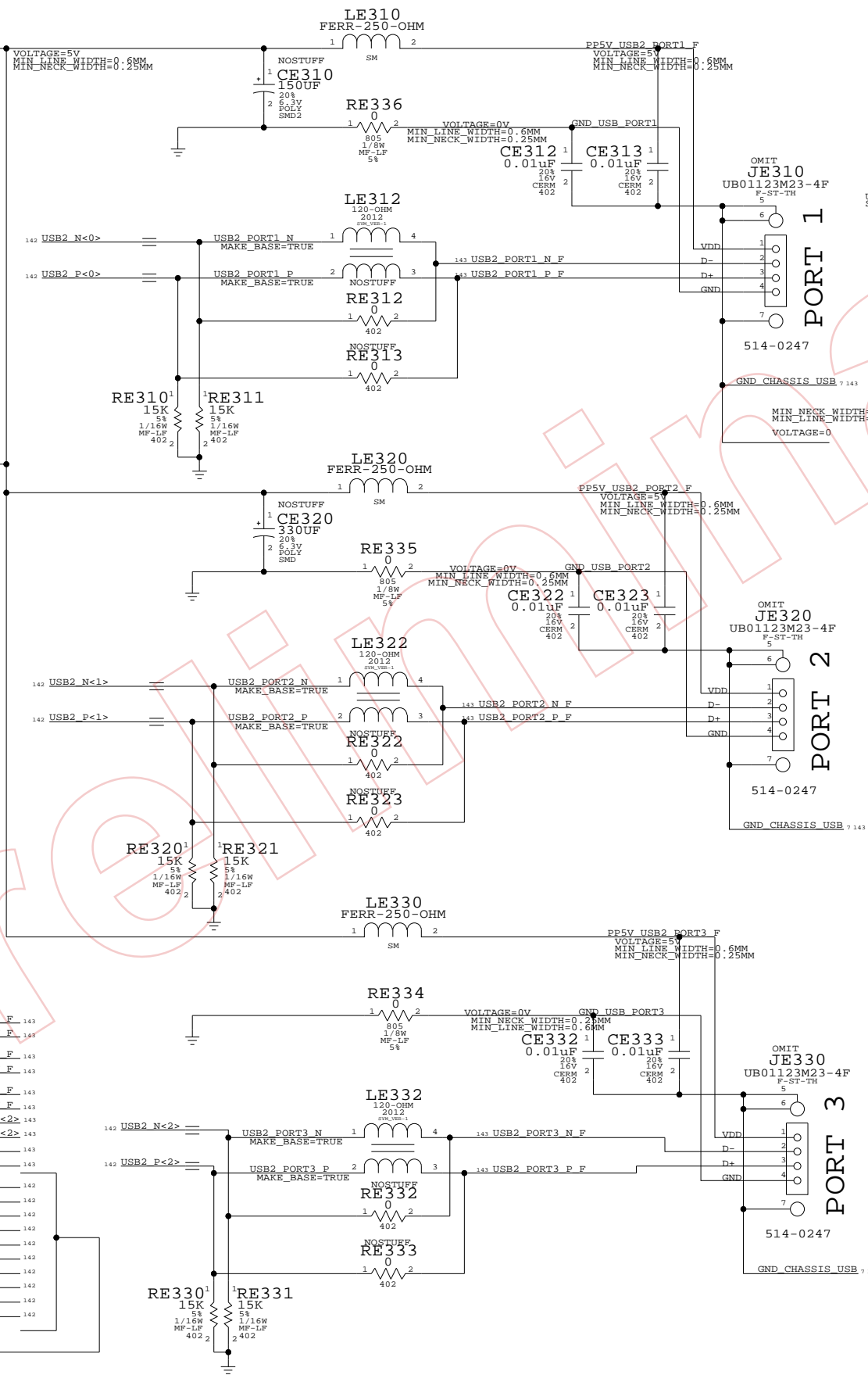


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0247	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0250	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

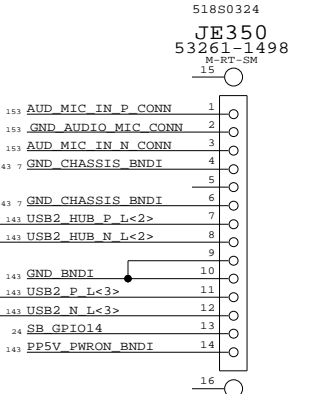
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE
PROVIDED BY	USB2	USB2_PORT1_P	USB2
USB CONTROLLER	USB2	USB2_PORT1_F	USB2
	USB2	USB2_PORT2_P	USB2
	USB2	USB2_PORT2_F	USB2
	USB2	USB2_PORT3_P	USB2
	USB2	USB2_PORT3_F	USB2
	USB2	USB2_HUB_P	USB2
	USB2	USB2_HUB_F	USB2
	USB2	USB2_BNDI_F	USB2
	USB2	USB2_BNDI_F	USB2
	USB2	USB2_0_IC	USB2
	USB2	USB2_0_IC	USB2
	USB2	USB2_1_IC	USB2
	USB2	USB2_1_IC	USB2
	USB2	USB2_2_IC	USB2
	USB2	USB2_2_IC	USB2
	USB2	USB2_3_IC	USB2
	USB2	USB2_3_IC	USB2
	USB2	USB2_4_IC	USB2
	USB2	USB2_4_IC	USB2

DUE TO THESE NETS ARE ON A Q63 SHARED PAGE 124, THESE PROPERTIES FOR M23/M33 WERE PLACED ON THIS PAGE.

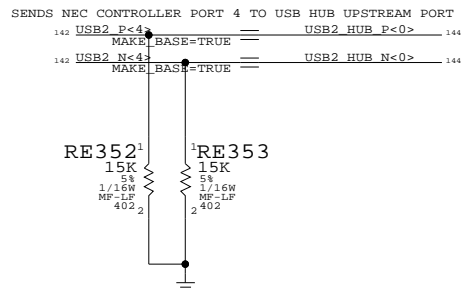
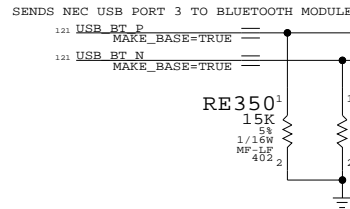
External USB Ports



FHB CONNECTOR



4-14-05
PLACE CE343, CE344 & LE340
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.



USB Device Interfaces

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

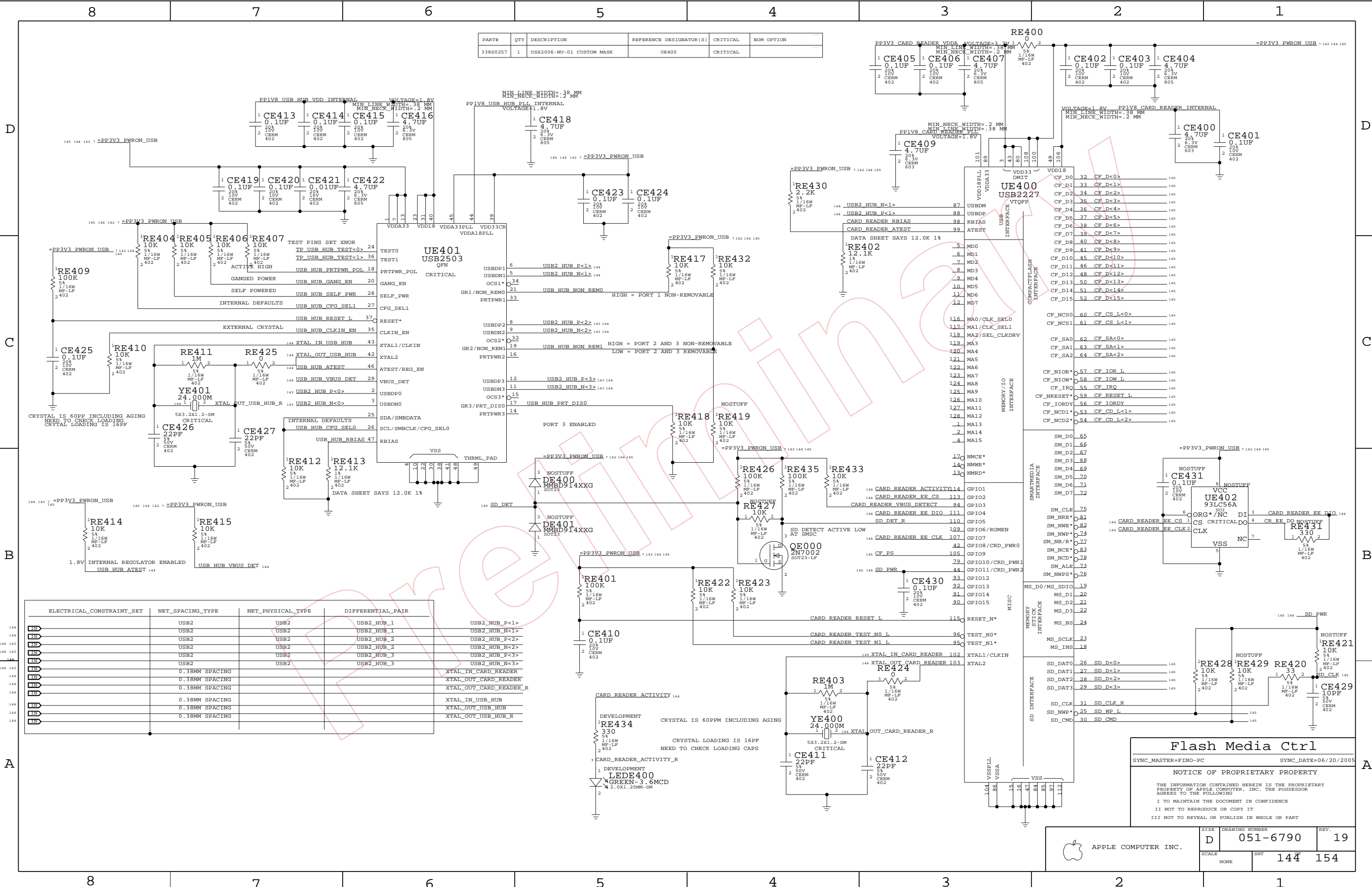
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	19
SCALE	SHT	OF
NONE	143	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0257	1	USX2006-NU-01 CUSTOM MASK	UE400	CRITICAL	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
144	USB2	USB2	USB2_HUB_1
144	USB2	USB2	USB2_HUB_2
144	USB2	USB2	USB2_HUB_3
144	USB2	USB2	USB2_HUB_4
144	USB2	USB2	USB2_HUB_5
144	USB2	USB2	USB2_HUB_6
144	USB2	USB2	USB2_HUB_7
144	USB2	USB2	USB2_HUB_8
144	USB2	USB2	USB2_HUB_9
144	USB2	USB2	USB2_HUB_10
144	USB2	USB2	USB2_HUB_11
144	USB2	USB2	USB2_HUB_12
144	USB2	USB2	USB2_HUB_13
144	USB2	USB2	USB2_HUB_14
144	USB2	USB2	USB2_HUB_15
144	USB2	USB2	USB2_HUB_16
144	USB2	USB2	USB2_HUB_17
144	USB2	USB2	USB2_HUB_18
144	USB2	USB2	USB2_HUB_19
144	USB2	USB2	USB2_HUB_20
144	USB2	USB2	USB2_HUB_21
144	USB2	USB2	USB2_HUB_22
144	USB2	USB2	USB2_HUB_23
144	USB2	USB2	USB2_HUB_24
144	USB2	USB2	USB2_HUB_25
144	USB2	USB2	USB2_HUB_26
144	USB2	USB2	USB2_HUB_27
144	USB2	USB2	USB2_HUB_28
144	USB2	USB2	USB2_HUB_29
144	USB2	USB2	USB2_HUB_30
144	USB2	USB2	USB2_HUB_31
144	USB2	USB2	USB2_HUB_32
144	USB2	USB2	USB2_HUB_33
144	USB2	USB2	USB2_HUB_34
144	USB2	USB2	USB2_HUB_35
144	USB2	USB2	USB2_HUB_36
144	USB2	USB2	USB2_HUB_37
144	USB2	USB2	USB2_HUB_38
144	USB2	USB2	USB2_HUB_39
144	USB2	USB2	USB2_HUB_40
144	USB2	USB2	USB2_HUB_41
144	USB2	USB2	USB2_HUB_42
144	USB2	USB2	USB2_HUB_43
144	USB2	USB2	USB2_HUB_44
144	USB2	USB2	USB2_HUB_45
144	USB2	USB2	USB2_HUB_46
144	USB2	USB2	USB2_HUB_47
144	USB2	USB2	USB2_HUB_48
144	USB2	USB2	USB2_HUB_49
144	USB2	USB2	USB2_HUB_50
144	USB2	USB2	USB2_HUB_51
144	USB2	USB2	USB2_HUB_52
144	USB2	USB2	USB2_HUB_53
144	USB2	USB2	USB2_HUB_54
144	USB2	USB2	USB2_HUB_55
144	USB2	USB2	USB2_HUB_56
144	USB2	USB2	USB2_HUB_57
144	USB2	USB2	USB2_HUB_58
144	USB2	USB2	USB2_HUB_59
144	USB2	USB2	USB2_HUB_60
144	USB2	USB2	USB2_HUB_61
144	USB2	USB2	USB2_HUB_62
144	USB2	USB2	USB2_HUB_63
144	USB2	USB2	USB2_HUB_64
144	USB2	USB2	USB2_HUB_65
144	USB2	USB2	USB2_HUB_66
144	USB2	USB2	USB2_HUB_67
144	USB2	USB2	USB2_HUB_68
144	USB2	USB2	USB2_HUB_69
144	USB2	USB2	USB2_HUB_70
144	USB2	USB2	USB2_HUB_71
144	USB2	USB2	USB2_HUB_72
144	USB2	USB2	USB2_HUB_73
144	USB2	USB2	USB2_HUB_74
144	USB2	USB2	USB2_HUB_75
144	USB2	USB2	USB2_HUB_76
144	USB2	USB2	USB2_HUB_77
144	USB2	USB2	USB2_HUB_78
144	USB2	USB2	USB2_HUB_79
144	USB2	USB2	USB2_HUB_80
144	USB2	USB2	USB2_HUB_81
144	USB2	USB2	USB2_HUB_82
144	USB2	USB2	USB2_HUB_83
144	USB2	USB2	USB2_HUB_84
144	USB2	USB2	USB2_HUB_85
144	USB2	USB2	USB2_HUB_86
144	USB2	USB2	USB2_HUB_87
144	USB2	USB2	USB2_HUB_88
144	USB2	USB2	USB2_HUB_89
144	USB2	USB2	USB2_HUB_90
144	USB2	USB2	USB2_HUB_91
144	USB2	USB2	USB2_HUB_92
144	USB2	USB2	USB2_HUB_93
144	USB2	USB2	USB2_HUB_94
144	USB2	USB2	USB2_HUB_95
144	USB2	USB2	USB2_HUB_96
144	USB2	USB2	USB2_HUB_97
144	USB2	USB2	USB2_HUB_98
144	USB2	USB2	USB2_HUB_99
144	USB2	USB2	USB2_HUB_100

Flash Media Ctrl

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

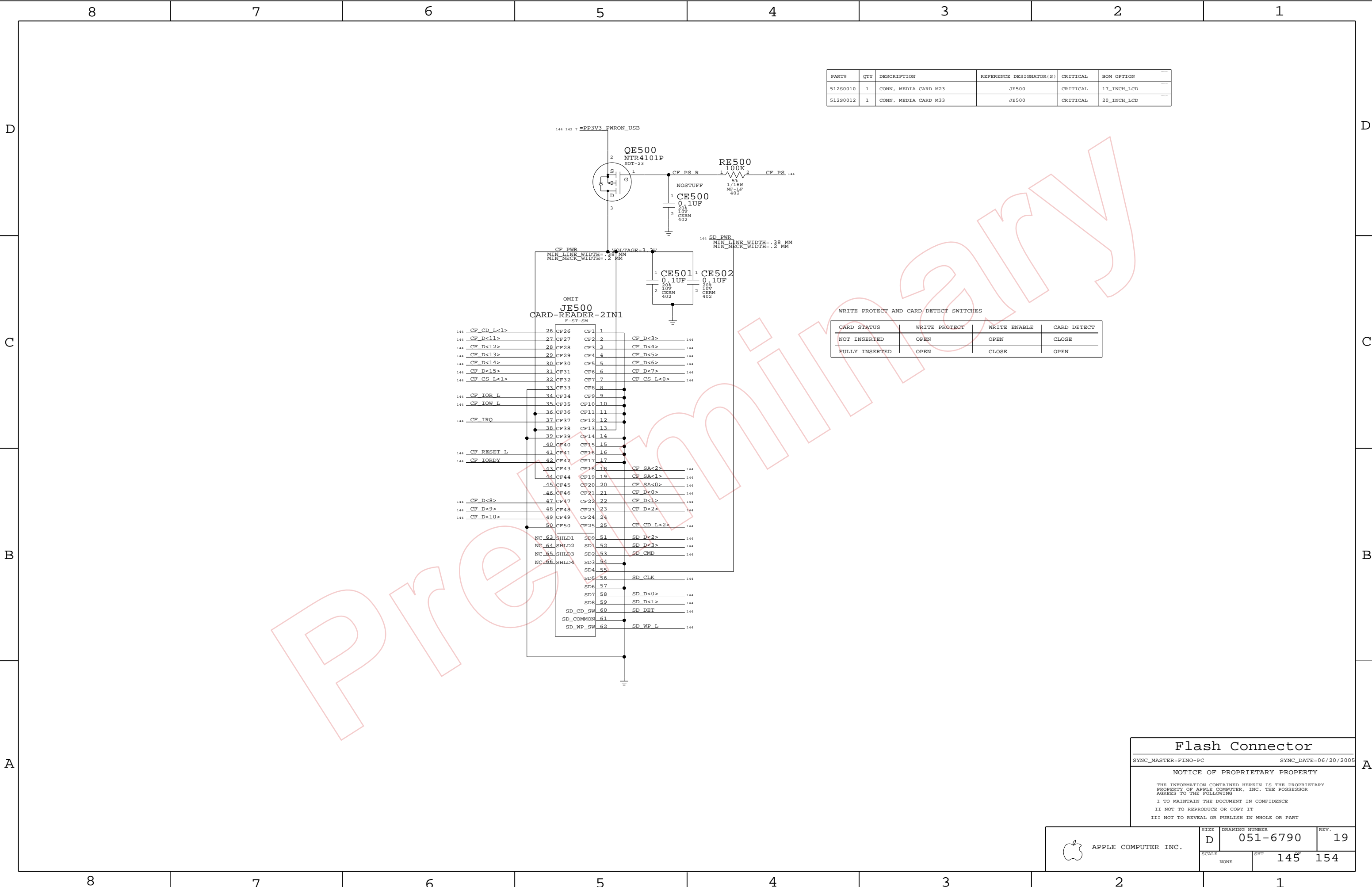
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51280010	1	CONN, MEDIA CARD M23	JE500	CRITICAL	17_INCH_LCD
51280012	1	CONN, MEDIA CARD M33	JE500	CRITICAL	20_INCH_LCD

WRITE PROTECT AND CARD DETECT SWITCHES			
CARD STATUS	WRITE PROTECT	WRITE ENABLE	CARD DETECT
NOT INSERTED	OPEN	OPEN	CLOSE
FULLY INSERTED	OPEN	CLOSE	OPEN

Flash Connector

SYNC_MASTER=FINO-PCSYNC_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	
NONE		145	154

D

C

B

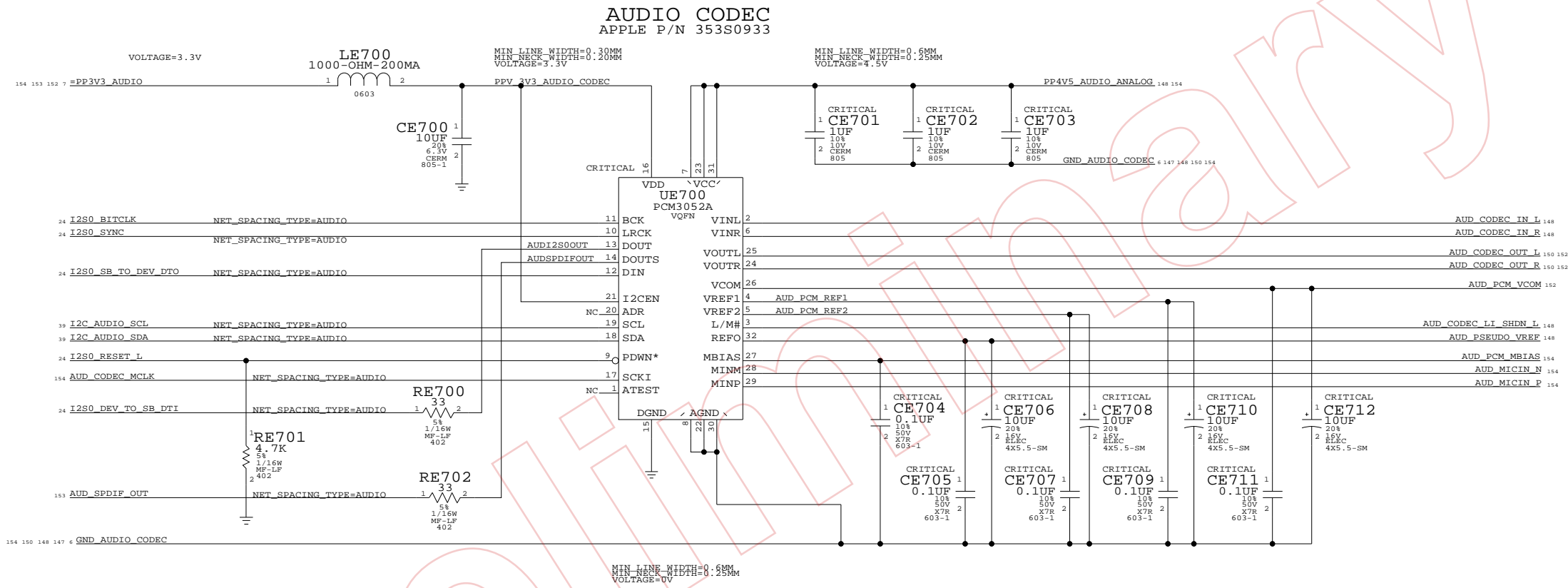
A

D


C

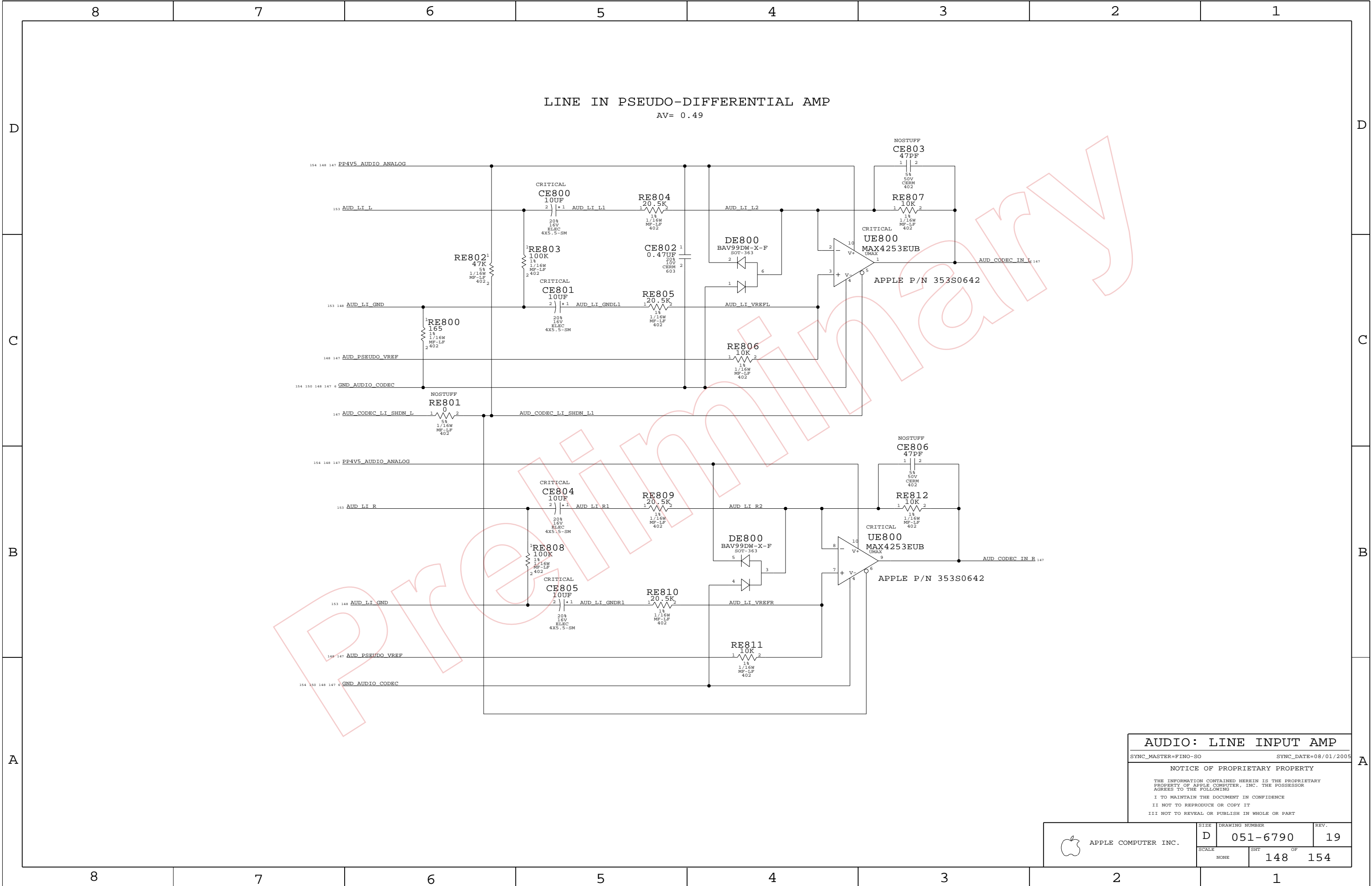
B

A



AUDIO: CODEC		
SYNC_MASTER=FINO-SO		SYNC_DATE=08/01/2005
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. 19
	SCALE NONE	SHT 147	OF 154



AUDIO: LINE INPUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=08/01/2005

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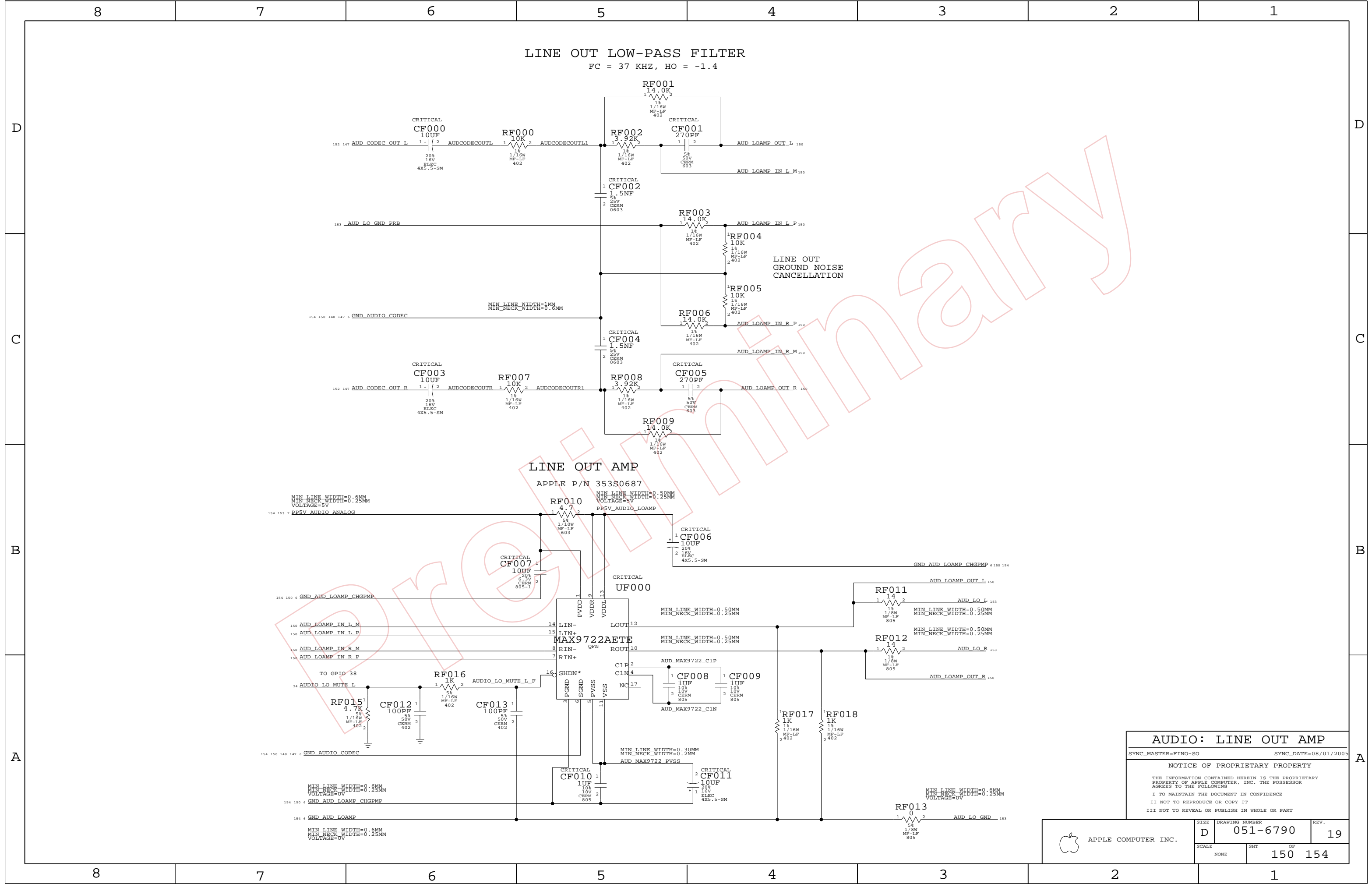
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	19
SCALE	SHT	OF
NONE	148	154



AUDIO: LINE OUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

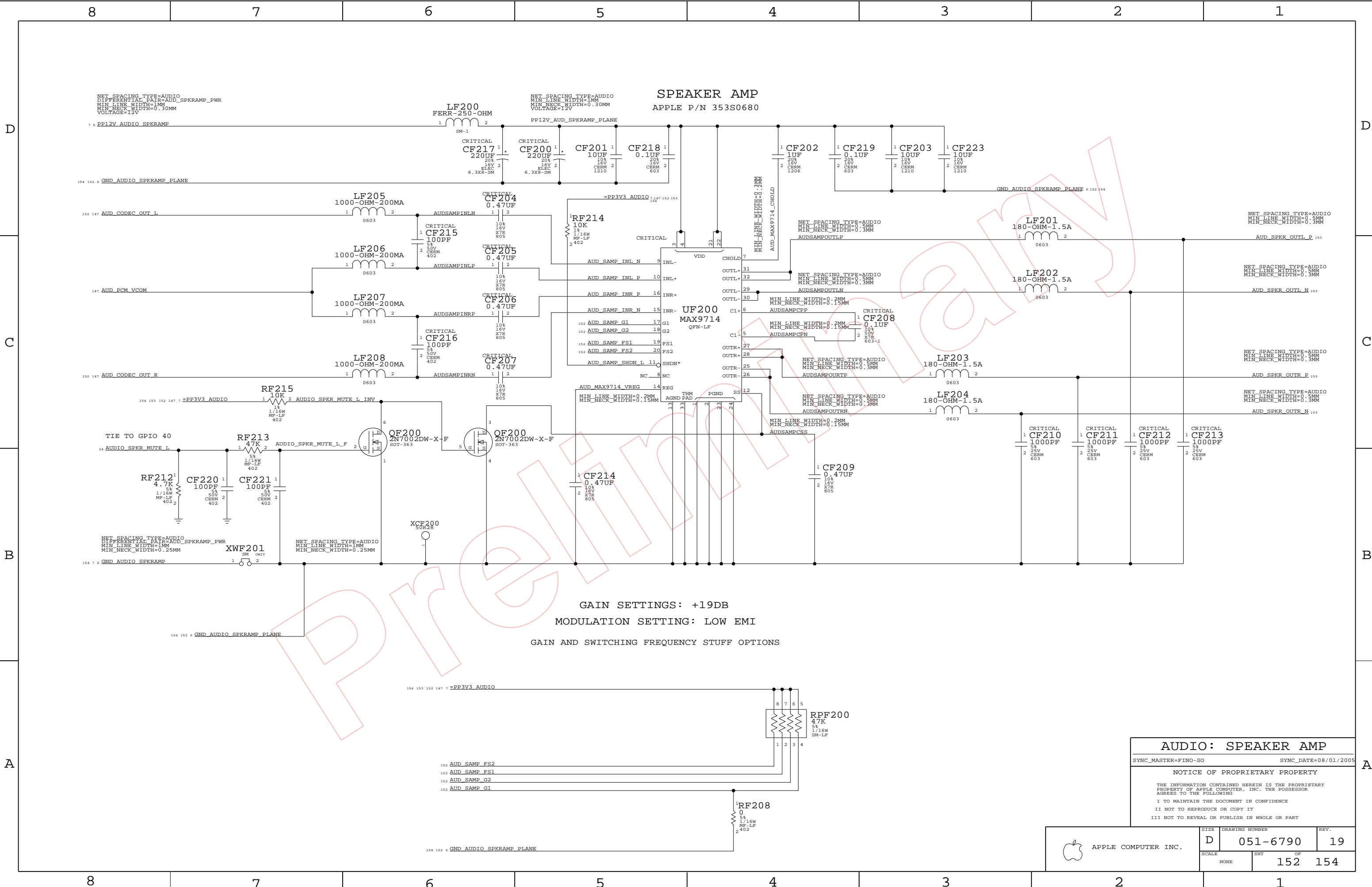
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE		SHT	OF
NONE		150	154

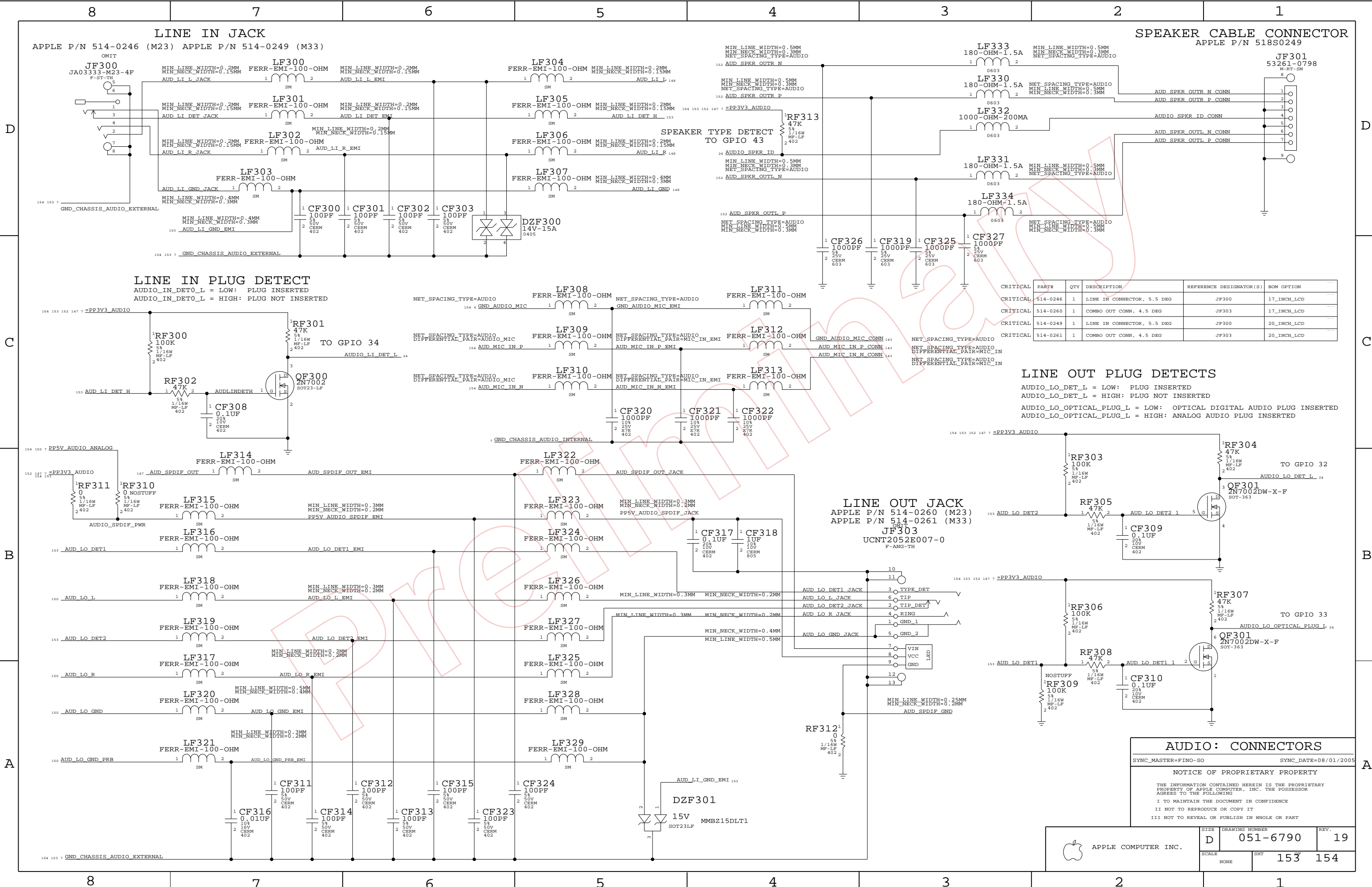


GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=FINO-SO SYNC_DATE=08/01/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE	SHT		OF
	NONE		152 154

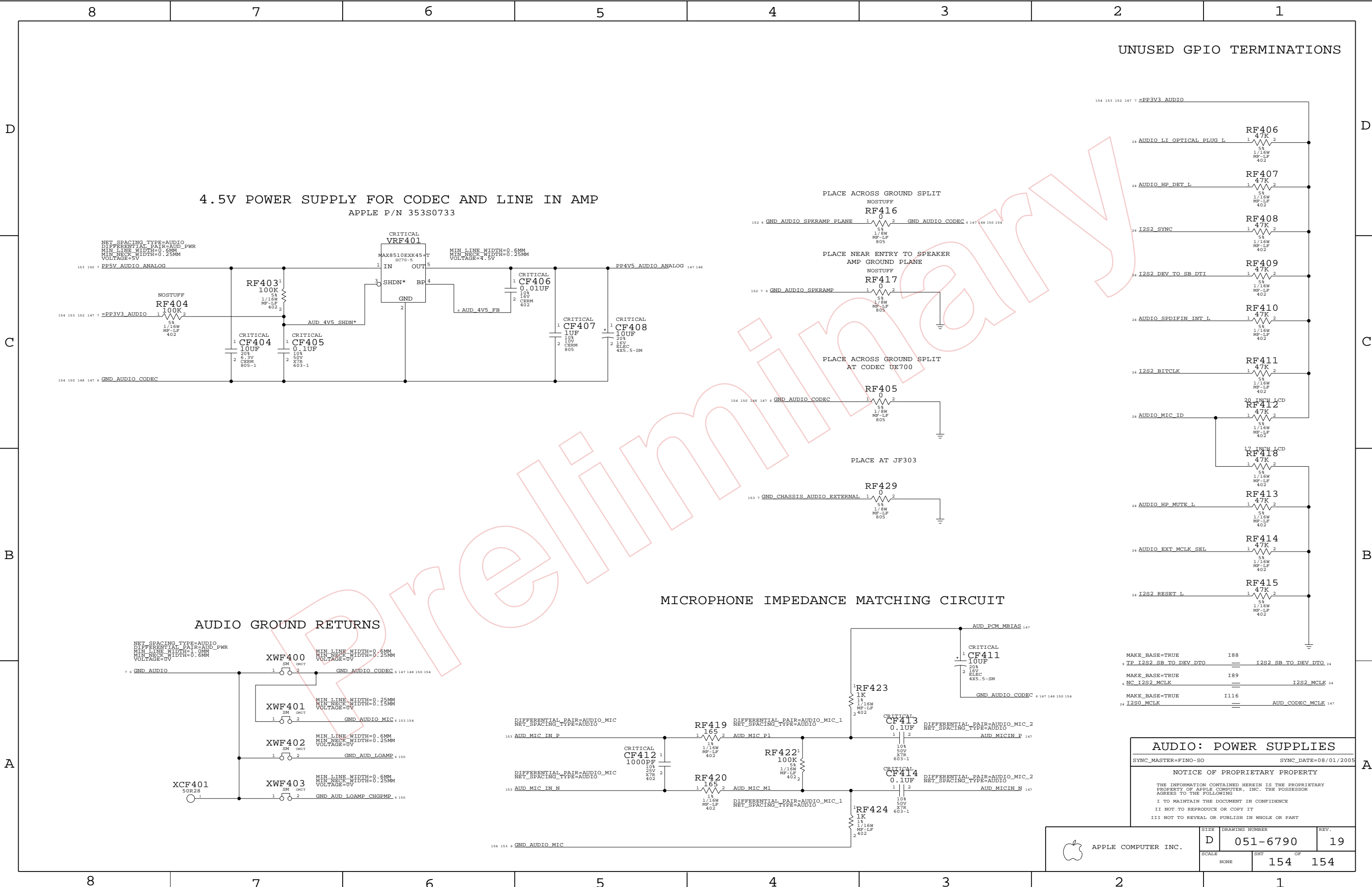


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE OUT PLUG DETECTS
AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED
AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED

AUDIO: CONNECTORS
SYNC_MASTER=FINO-SO SYNC_DATE=08/01/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	19
SCALE	SHT	153	154
NONE			



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APPLE P/N 353S0733

MICROPHONE IMPEDANCE MATCHING CIRCUIT

AUDIO GROUND RETURNS

UNUSED GPIO TERMINATIONS

AUDIO: POWER SUPPLIES

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	D	051-6790	19
SCALE	NONE		OF
	154		154